

# BAD50\_HC

## DIS/UMA/Muxless Schematics Document

### IVY/SNB Bridge

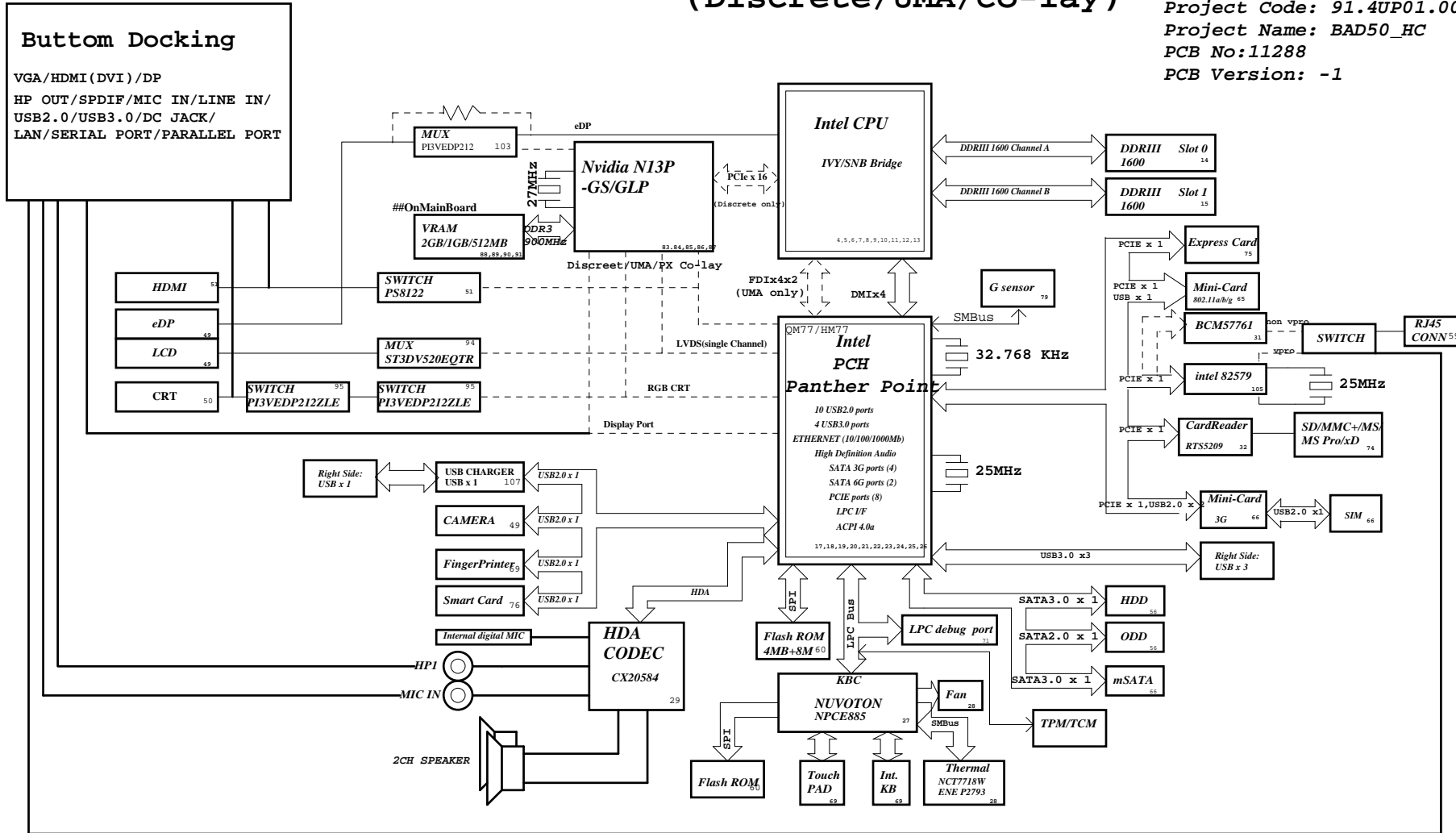
### Panther Point

*DY :None Installed*  
*DIS:DIS installed*  
*DIS\_Muxless :BOTH DIS or Muxless installed*  
*DIS\_PX:BOTH DIS or PX installed*  
*DIS\_PX\_Muxless:DIS or PX or Muxless installed.*  
*Muxless: Muxless installed.(PX4.0)*  
*PX:MUX installed.(PX3.0)*  
*PX\_Muxless:BOTH PX or Muxless installed.*  
*UMA:UMA installed*  
*UMA\_Muxless:BOTH UMA or Muxless installed*  
*UMA\_PX\_Muxless:UMA or PX or Muxless installed*

*ANNIE: ONLY FOR ANNIE solution.*  
*PSL: KBC885 PSL circuit for 10mW solution installed.*  
*10mW: External circuit for 10mW solution installed.*  
*65W: for 65W adaptor installed.*  
*90W: for 90W adaptor installed.*

## BAD50-HC Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4UP01.001  
Project Name: BAD50\_HC  
PCB No:11288  
PCB Version: -1



TI CHARGER		40
BQ24707		
INPUTS	DCBATOUT	
OUTPUTS	BT+	
SYSTEM DC/DC		
RT8239CGWV		41
INPUTS	DCBATOUT	
OUTPUTS	5V_AUX_85 3D3V_AUX_85 5V_CHARGER 3D3V_85	
CPU DC/DC		
ISL95831HRTZ		42-43
INPUTS	DCBATOUT	
OUTPUTS	VCC_CORE	
GFX DC/DC		
ISL95831HRTZ		44
INPUTS	DCBATOUT	
OUTPUTS	+VCC_GFXCORE	
SYSTEM DC/DC		
TPS51218DS		45
INPUTS	DCBATOUT	
OUTPUTS	1D05V_LAN	
SYSTEM DC/DC		
RT8207LGWV		46
INPUTS	DCBATOUT	
OUTPUTS	1D5V_80 0D75V_80	
SYSTEM DC/DC		
APW7153B		47
INPUTS	3D3V_85	
OUTPUTS	1D8V_80	
SYSTEM DC/DC		
TPS51461		48
INPUTS	5V_85	
OUTPUTS	0D85V_80	
VGA		
VT1312MFXQ		92
INPUTS	5V_PWR	
OUTPUTS	VGA_CORE	
Switches		
INPUTS	OUTPUTS	
5V_CHARGER	5V_85	
Switches		
INPUTS	OUTPUTS	
1D5V_83	1D5V_VGA_80	
3D3V_80	3D3V_VGA_80	
PCB LAYER		
L1:Top	L5:Power	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

PCH Strapping Chief River Schematic Checklist Rev1.5

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> If the signal is sampled high.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high. External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor.
DF_TVS	A strap for selecting DMI and FDI termination voltage. DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms $\pm 5\%$ resistor.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts.
SATA2GP/ GPIO36	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_SDO	Weak internal pull-down. This signal has a 20k internal pull down resistor.
HDA_SYNC	On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality.
L_DDC_DATA	When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down
SDVO_CTRLDATA DDPC_CTRLDATA DDPD_CTRLDATA	When '1'- Port B is detected; When '0'- Port B is not detected This signal has a weak internal pull-down
DSWVRMEN	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	If not used, 8.2-k $\Omega$ to 10-k $\Omega$ pull-up to +V3.3A power-rail. GPIO28 signal also needs to be pulled up to 3.3V_SUS with 4.7K resistor to ensure proper strap setting when use as the chipset test interface.
GPIO29/ SLP_LAN#	If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN. If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO.

## USB Table

## PCIE Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN
LANE7	New Card
LANE8	X

## SATA Table

SATA	
Pair	Device
0	HDD1
1	M-SATA
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	USB port 1
1	USB port 2
2	USB port3 (usb charger)
3	Dock
4	X
5	Fingerprint
6	smart card
7	X
8	Mini Card2 (WWAN)
9	USB port4(ESATA ),on M/
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

# Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1 kOhms resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace.	
CFG[2]	PCIe Static x16 Lane Numbering Reversal	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed	1
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connect to the EMBEDDED display Port	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	1
CFG[17:7]	configuration lands. A test point may be placed on the board for these lands.		

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1.5V 1.05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_CHARGER 5V_AUX_S5 3D3V_S5	7V-19.5V 7V-19.5V 5V 5V 5V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_S5 3D3V_LAN_S5	3.3V 3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

## SMBus ADDRESSES

I <sup>2</sup> C / SMBus Addresses		CHIEF RIVER ORB	
Device		Address	Bus
EC SMBus 1			
Battery 0		0x16	BAT_SCL/BAT_SDA
CHARGER		0x12	BAT_SCL/BAT_SDA
P8B122 (HDMI Switch) (Bottom Dock)		0x9E	BAT_SCL/BAT_SDA
USB3.0 redriver P8B710 (Bottom Dock)		0x40	BAT_SCL/BAT_SDA
EC SMBus 2			
Battery 1		0x16	SMML_CLK/SMML_DATA
PCB		0x96 or 0x94	SMML_CLK/SMML_DATA
Discrete VDMA Thermal		0x9c or 0x9E	SMML_CLK/SMML_DATA
P8B321 HDMI level shifter		0x96 or 0x97	SMML_CLK/SMML_DATA
NCT771BW		0x98 or 0x99	SMML_CLK/SMML_DATA
EC SMBus 3			
NCT5605Y-0		0x30	SMB2_CLK/SMB2_DATA
NCT5605Y-1		0x32	SMB2_CLK/SMB2_DATA
PCB SMBus			
SO-DIMM0			PCB_SMBDATA/PCB_SMBCLK
SO-DIMM0			PCB_SMBDATA/PCB_SMBCLK
Intel LAN 82579			PCB_SMBDATA/PCB_SMBCLK
G-Sensor			PCB_SMBDATA/PCB_SMBCLK
NI WWAN			PCB_SMBDATA/PCB_SMBCLK
Intel LAN82579			PCB_SMBDATA/PCB_SMBCLK

### <Core Design>

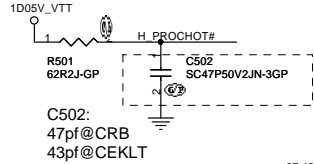
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

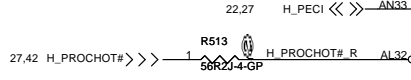
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Size A3	Document Number	Rev	
	<b>BAD50-HC</b>	<b>-1</b>	
Date:	Friday, March 02, 2012	Sheet 3 of	109



SSID = CPU

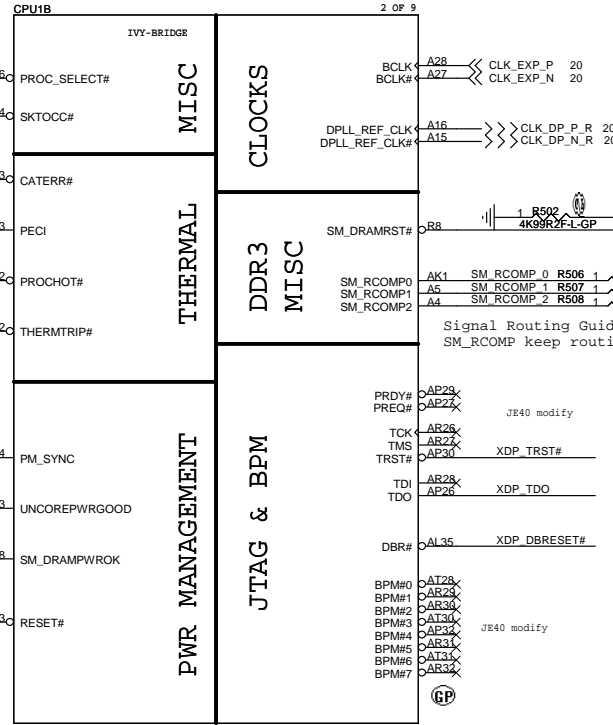
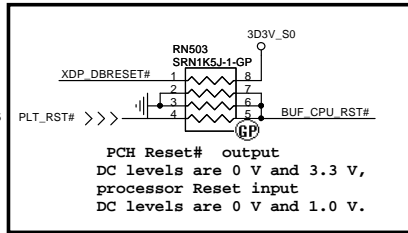
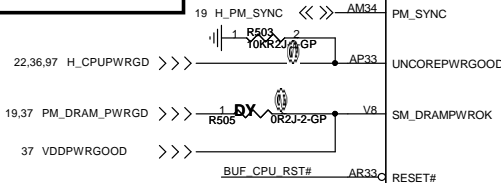


CATERR#  
this signal should have  
an exposed test point for  
easy debug access.



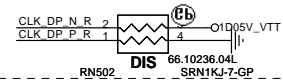
Connect EC to PROCHOT# through inverting OD buffer.

PROCHOT# with Two VR topology:  
Requires a series-resistor of 100  $\pm 5\%$   
close to the processor followed by a  
75  $\pm 5\%$  pull-up to VTT power-rail towards the VR.  
A pull up to VCCP(1.05 V)  
through 300  $\pm 5\%$  resistor close to the IMVP 7

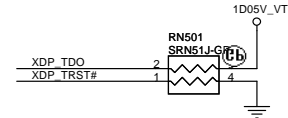


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Disabling Guidelines:  
If motherboard only supports external graphics:  
Connect DPLL\_REF\_SSCLK on Processor to GND through  
1K +/- 5% resistor.  
Connect DPLL\_REF\_SSCLK# on Processor to VCCP  
through 1K +/- 5% resistor power (~15 mW) may be  
wasted.



Signal Routing Guideline:  
SM\_RCOMP keep routing length less than 500 mils.

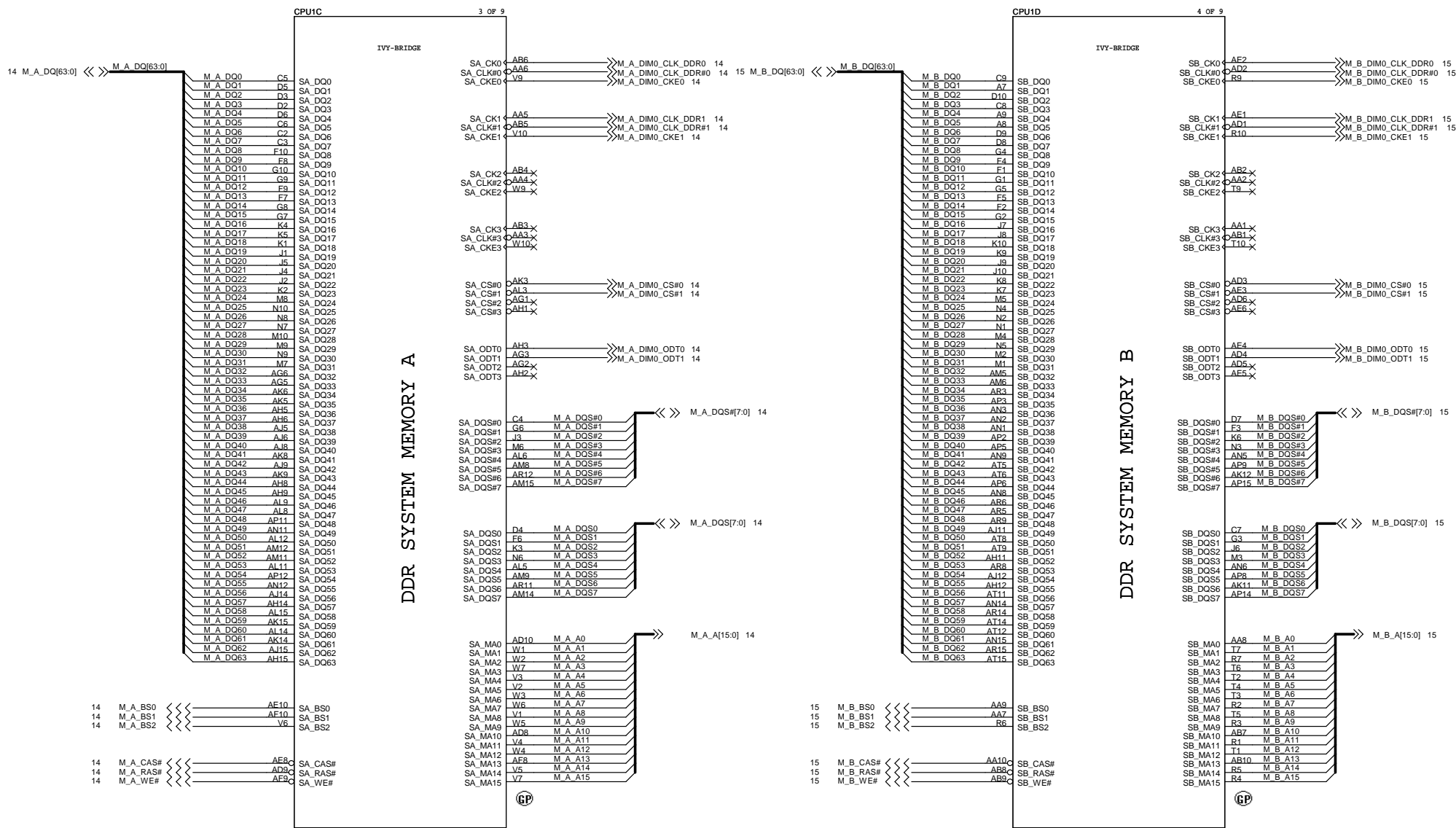


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Title	CPU (THERMAL/CLOCK/PM)	
Size	Document Number	Rev
Custom	BAD50-HC	-1
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www.vinafix.vn

SSID = CPU
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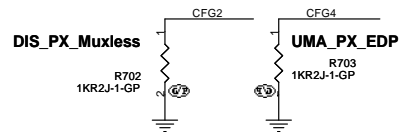
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Title			
<b>CPU (DDR)</b>			
Size A3	Document Number		Rev
	<b>BAD50-HC</b>		<b>-1</b>
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SSID = CPU



PEG Static Lane Reversal

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

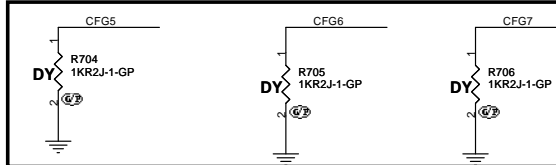
PCIe Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

SA



Configuration Straps

The CFG straps have a default value of 0. If not mentioned on the board, refer to the Chip Power System Design Guide for pull down recommendations when a logic low is desired.

CFG[1:0]: Reserved configuration lanes. A test point may be placed on the board for this area.

CFG[2]: PCI Express Static x16 Lane Number Reversal

1: Normal Operation

0: Lane numbers reversed

CFG[3]: Reserved

CFG[4]: PEG enable

1: Disabled

0: Enabled

CFG[5:3]: PCI Express Bifurcation

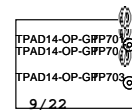
00: x16, x8, 2 x4 PCI Express

01: Reserved

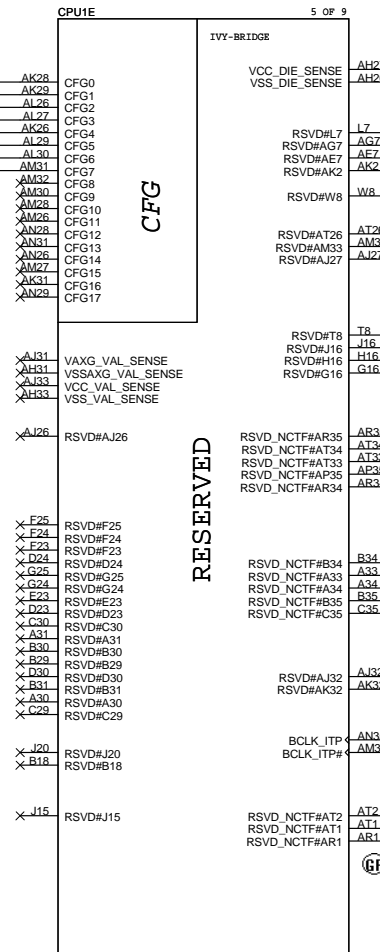
10: 2 x8 PCI Express

11: 1 x16 PCI Express

CFG[7:2]: Reserved configuration lanes. A test point may be placed on the board for these straps.



1	CFG0	AK28
1	CFG1	AK29
1	CFG2	AL26
1	CFG3	AL27
1	CFG4	AK26
1	CFG5	AL29
1	CFG6	AL30
1	CFG7	AM31

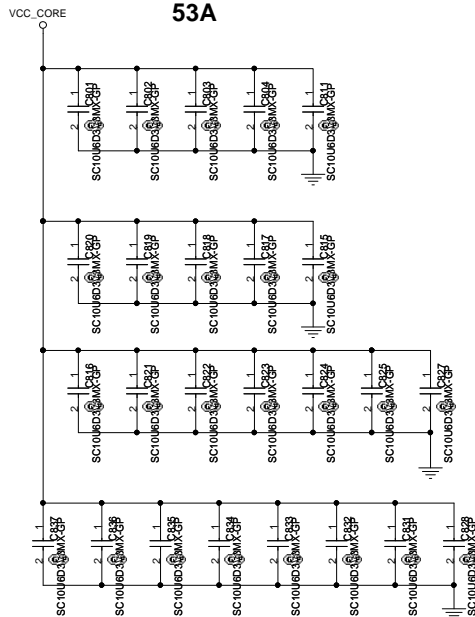




SSID = CPU

# PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:  
4 x 470 uF at Bottom Socket Edge  
8 x 22 uF at Top Socket Cavity  
8 x 22 uF at Top Socket Edge  
8 x 22 uF at Bottom Socket Cavity

# POWER

CPU1F

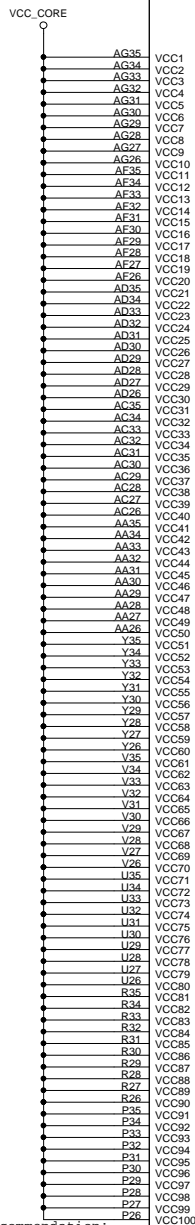
6 OF 9

IVY-BRIDGE

PEG AND DDR

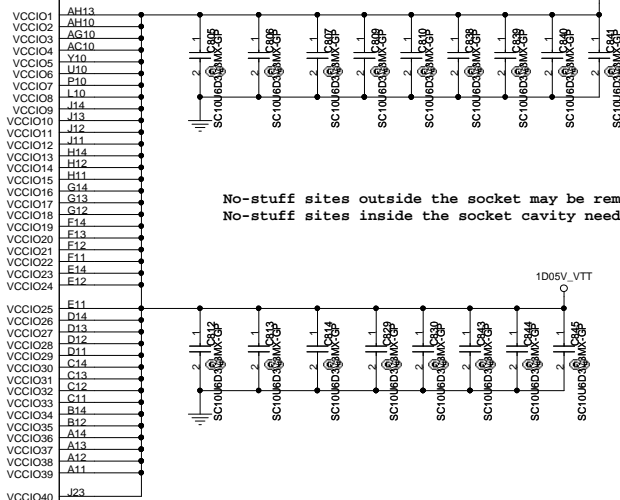
SVID

SENSE LINES



VCCIO Output Decoupling Recommendation:  
2 x 330 uF (3 x 330 uF for 2012 capable designs)  
5 x 22 uF & 5 x 0805 no-stuff at Bottom  
7 x 22 uF & 2 x 0805 no-stuff at Top

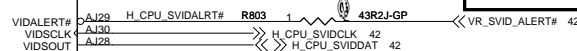
No-stuff sites outside the socket may be removed.  
No-stuff sites inside the socket cavity need to remain.



close to CPU

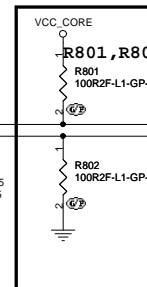
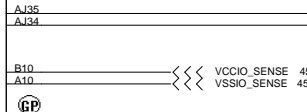
H\_CPU\_SVIDDRT# R803 1 43R2J-GP

PR4201 PU



VCC\_SENSE  
VSS\_SENSE

VCCIO\_SENSE  
VSS\_SENSE\_VCCIO



close to CPU

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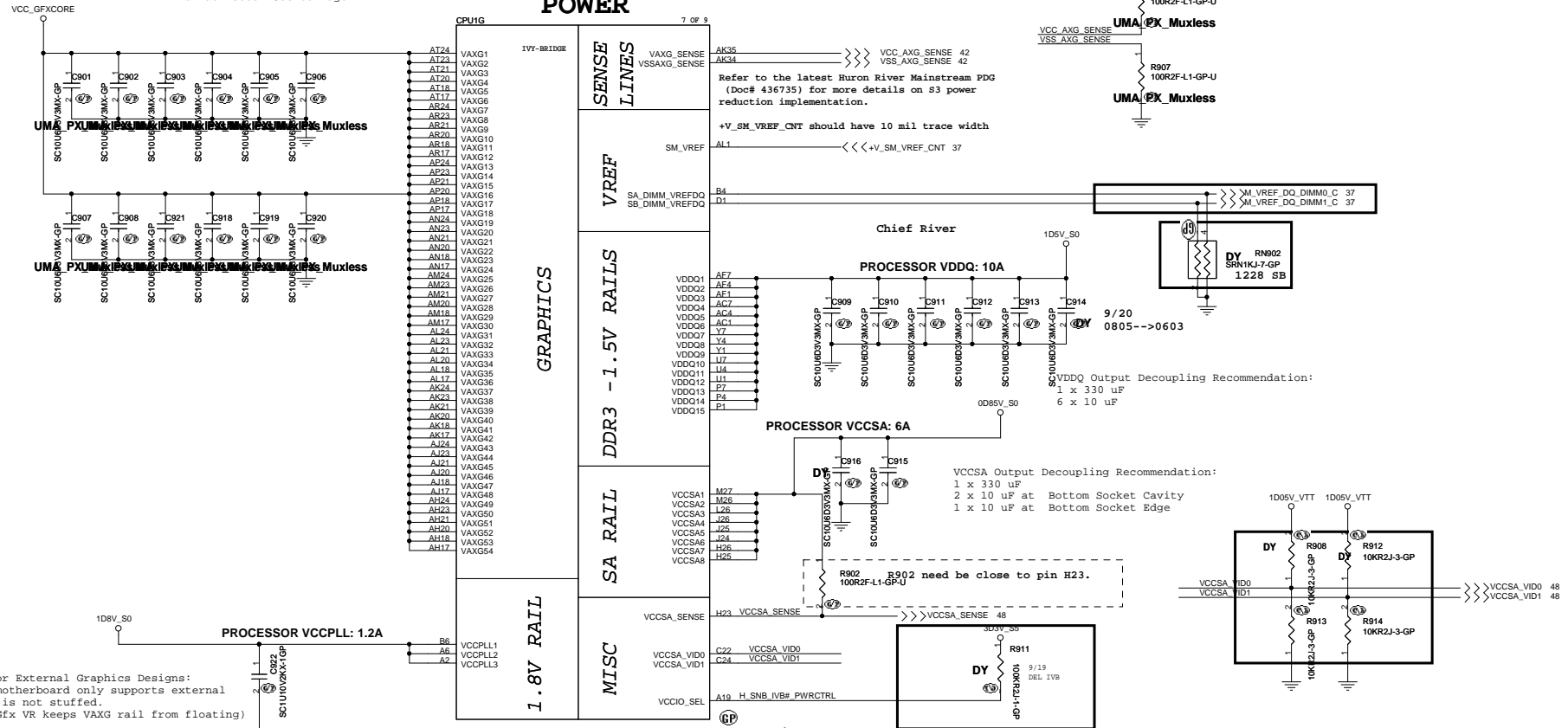
CPU (VCC CORE)		
Size	Document Number	Rev
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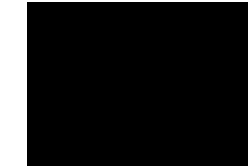
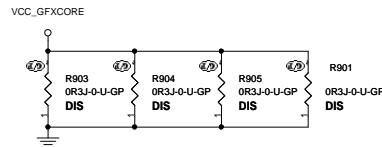
SSID = CPU

VAXG Output Decoupling Recommendation:  
2 x 470 uF at Bottom Socket Edge  
2 x 22 uF at Top Socket Cavity  
4 x 22 uF at Top Socket Edge  
2 x 22 uF at Bottom Socket Cavity  
4 x 22 uF at Bottom Socket Edge

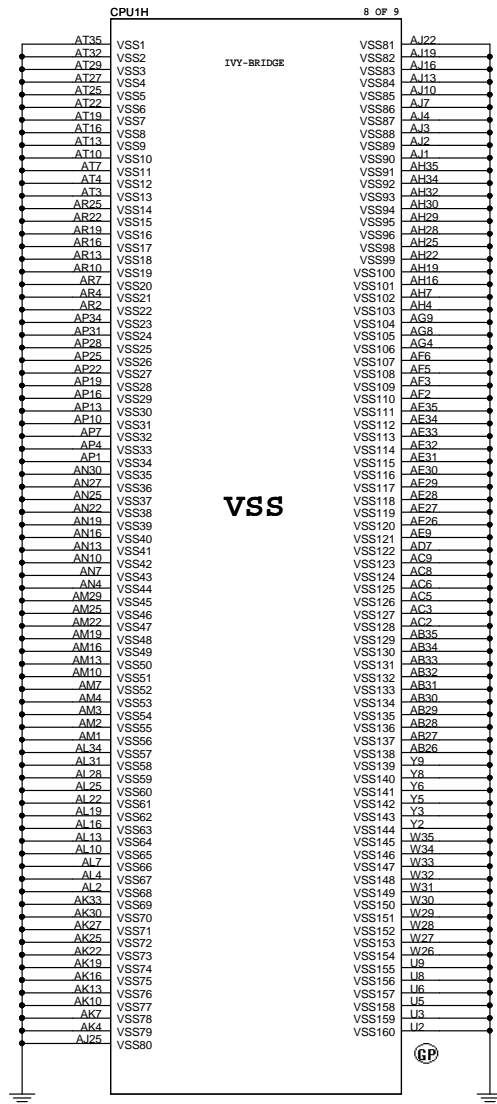
R906,R907 close to CPU



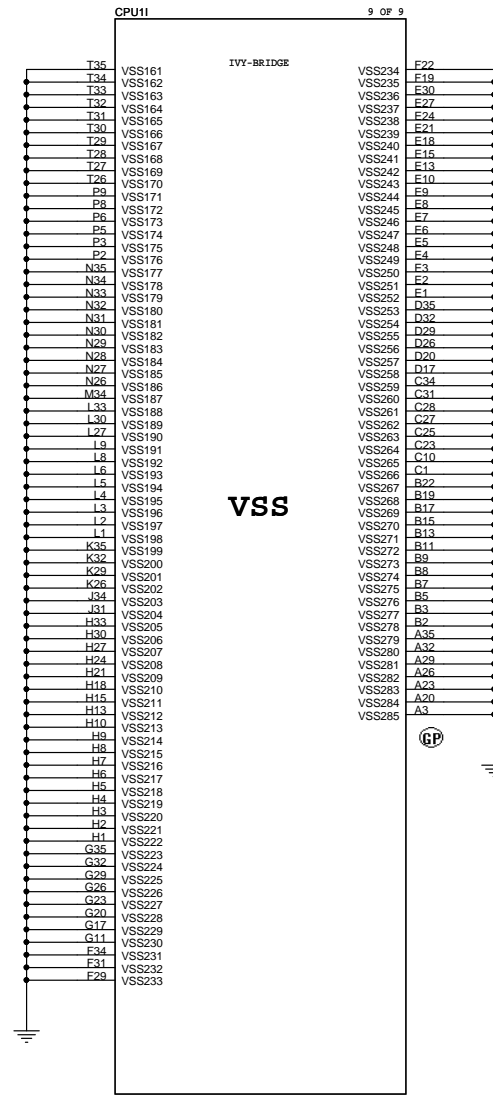
Disabling Guidelines for External Graphics Designs:  
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.  
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed



SSID = CPU



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<Core Design>

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Title

CPU (VSS)

Size

A3

Document Number

BAD50-HC

Rev

-1

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JE40 delete XDP function

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Title			
<b>XDP</b>			
Size	Document Number		Rev
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Title			
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Size A4	Document Number  BAD50-HC		Rev  -1
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Size	Document Number				Rev
A4	BAD50-HC				-1
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SSID = MEMORY

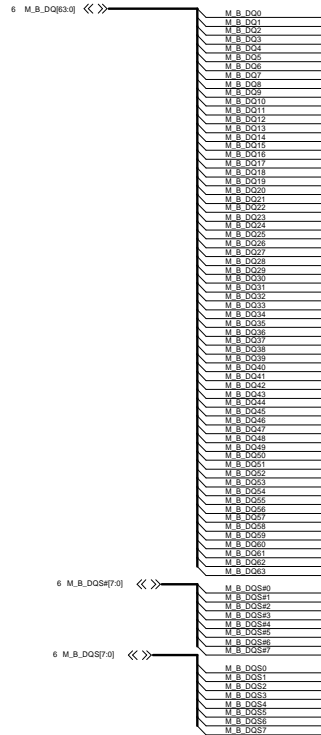
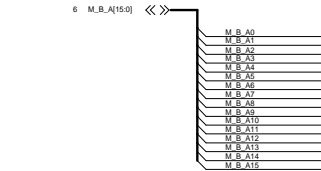
M\_A\_A[15:0] 6

M\_A\_BS2 >>>  
M\_A\_BS0 >>>  
M\_A\_BS1 >>>  
M\_A\_DQ[63:0] >>>

DM1  
M\_A\_A0 98  
M\_A\_A1 97  
M\_A\_A2 96  
M\_A\_A3 95  
M\_A\_A4 94  
M\_A\_A5 93  
M\_A\_A6 92  
M\_A\_A7 91  
M\_A\_A8 90  
M\_A\_A9 89  
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A16/BA2

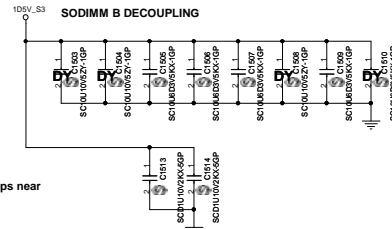
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M\_A\_DQ1 6  
M\_A\_DQ2 7  
M\_A\_DQ3 8  
M\_A\_DQ4 9  
M\_A\_DQ5 10  
M\_A\_DQ6 11  
M\_A\_DQ7 12  
M\_A\_DQ8 13  
M\_A\_DQ9 14  
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M\_A\_DQ42 47  
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M\_A\_DQS#753 12

SSID = MEMORY

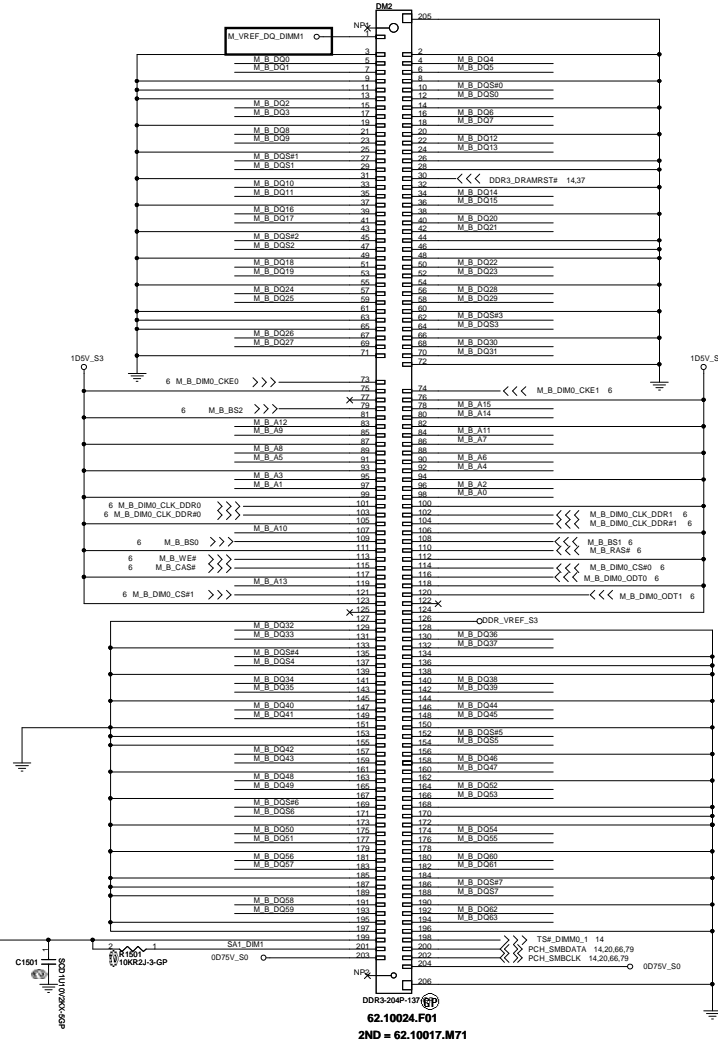
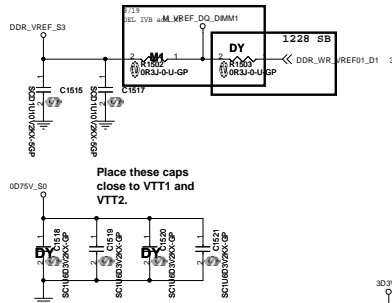


Note:  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from  
the Processor than SO-DIMMA



Layout Note:  
Place these Caps near  
SO-DIMMB.



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Core Design

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File  
Size A3  
Document Number  
Date: Thursday, March 28, 2012  
Sheet 16 of 109

DDR3-SODIMM2

BAD50-HC

Rev -1



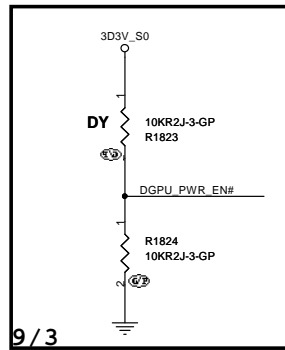
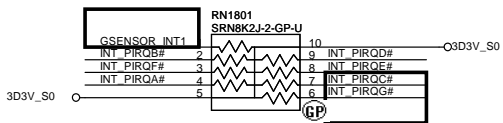
(Blanking)

<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>DDR3-SODIMM2</b>			
Size A4	Document Number <b>BAD50-HC</b>		Rev <b>-1</b>
Date:	Friday, March 02, 2012	Sheet 16	of 109

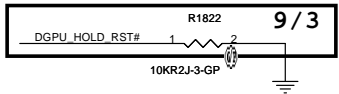


SSID = PCH



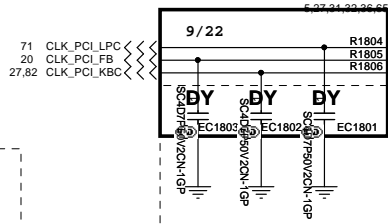
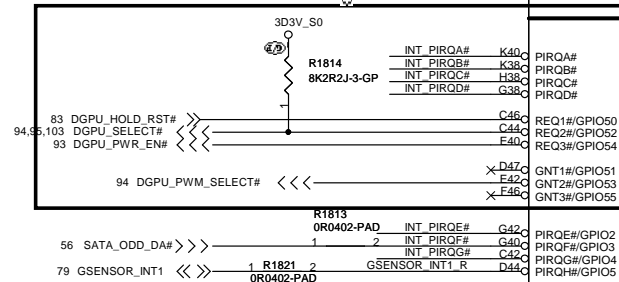
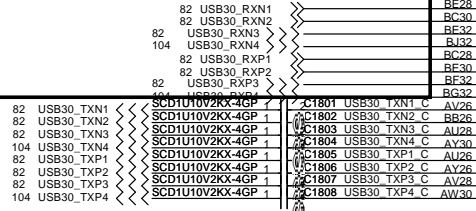
Al6 swap override Strap/Top-Block  
Swap Override jumper

PCI\_GNT#3 Low = Al6 swap  
override/Top-Block  
Swap Override enabled  
High = Default



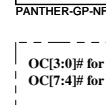
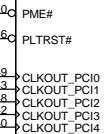
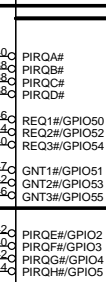
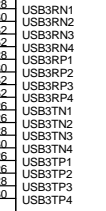
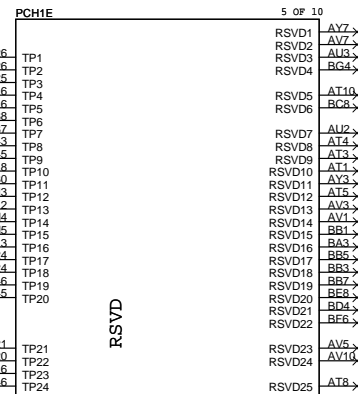
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

9/21 del USB REDRIVER



-1\_0303

EMI request 20101109



EMI request 20101109

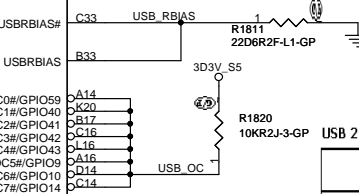
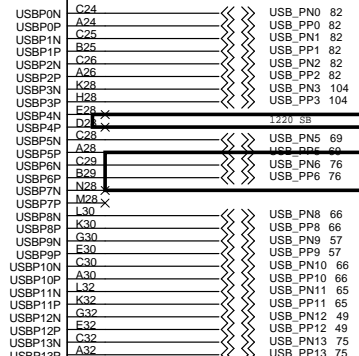
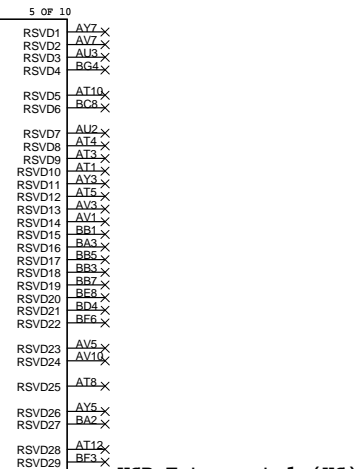
RSVD

USB

PCI

PANTHER-GP-NF

OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)

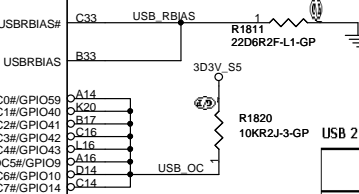


EMI request 20101109

USB Ext. port 1 (HS)  
External debug port use on Huron river platform

USB Table

Pair	Device
0	USB port 1
1	USB port 2
2	USB port3 (usb charger)
3	Dock
4	X
5	Fingerprint
6	smart card
7	X
8	Mini Card2 (WWAN)
9	USB port4(ESATA ),on M/B
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card



EMI request 20101109

USB 2.0 Overcurrent Pin Default Usage







Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used






<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (PCI/USB/NVRAM)			
Size	Document Number	Rev	
A3	BAD50-HC	-1	
Date:	Saturday, March 03, 2012	Sheet	18 of 109

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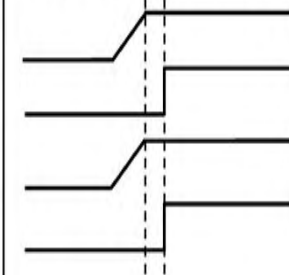
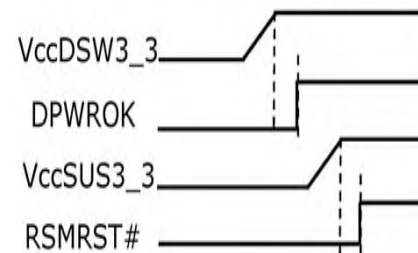
4 DMI\_RXN[3:0]        
4 DMI\_RXP[3:0]      

4 DMI\_TXN[3:0]        
4 DMI\_TXP[3:0]      

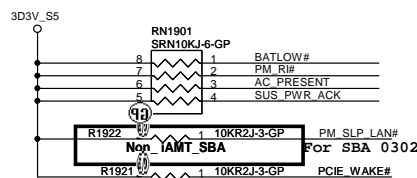
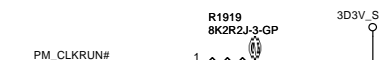
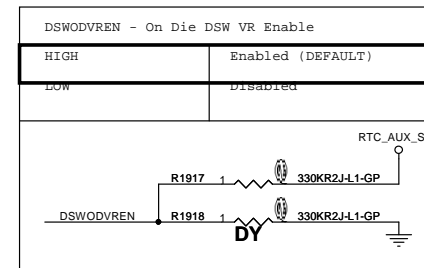
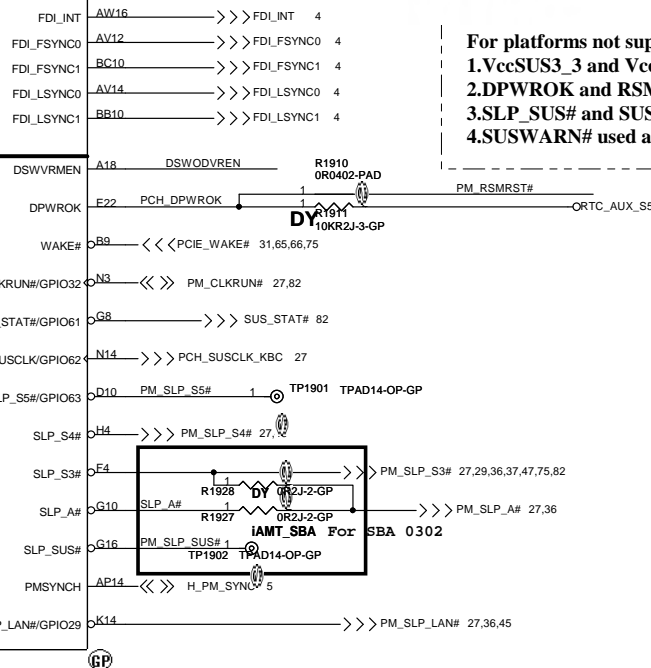
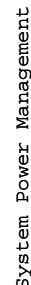
The diagram illustrates the DMI bus structure. It shows four groups of registers, each with a corresponding set of four bus lines. The registers are: DMI\_RXN0, DMI\_RXN1, DMI\_RXN2, DMI\_RXN3; DMI\_RXP0, DMI\_RXP1, DMI\_RXP2, DMI\_RXP3; DMI\_TXN0, DMI\_TXN1, DMI\_TXN2, DMI\_TXN3; and DMI\_TXP0, DMI\_TXP1, DMI\_TXP2, DMI\_TXP3. Each register is connected to its respective bus lines via a set of four wavy lines.



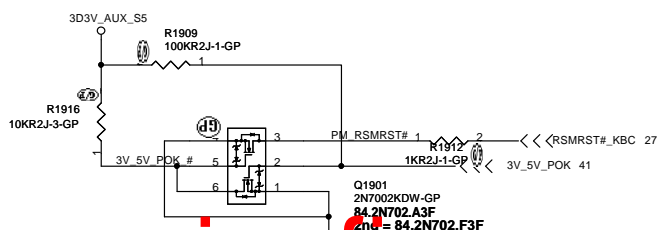
Deep S4/S5 **Not** Supported



- 1.VccSUS3\_3 and VccDSW3\_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP\_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30



```
PCIE_WAKE#
CRB : 1K
CEKLT: 10K
```



```
PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K
```

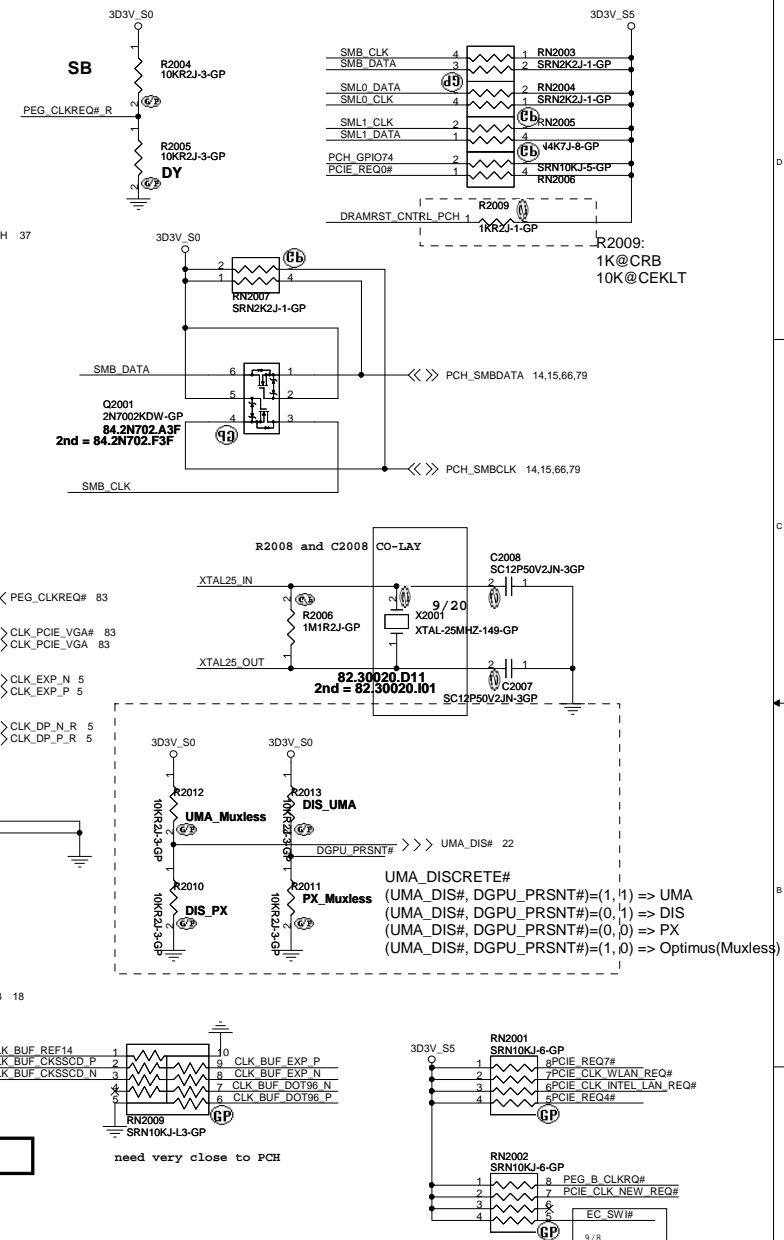
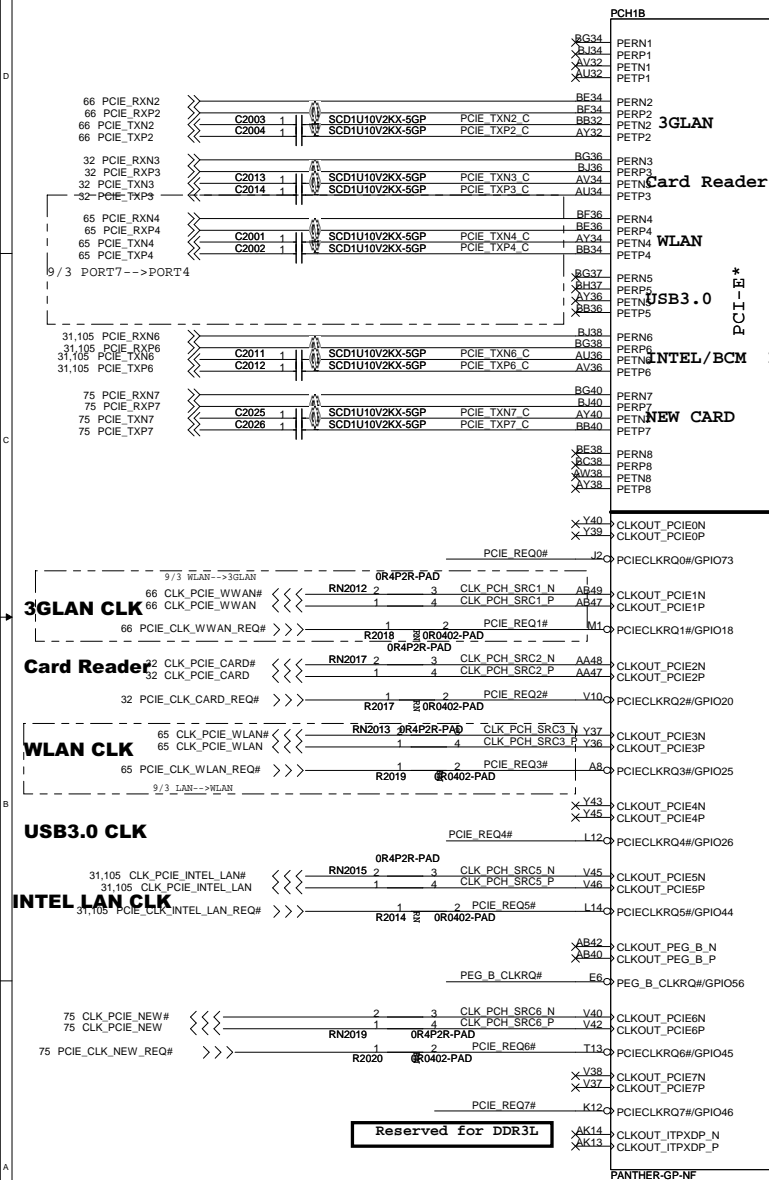
緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>PCH (DM I/FDI/PM)</b>
-------	--------------------------

Size A3	Document Number <b>BAD50-HC</b>	Rev <b>-1</b>
Date: Saturday, March 03, 2012	Sheet 19 of 109	

SSID = PCH



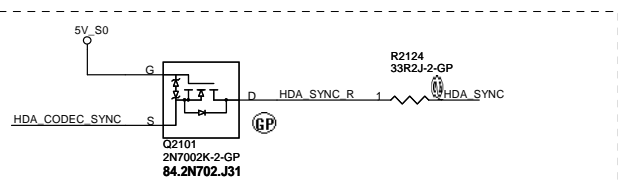
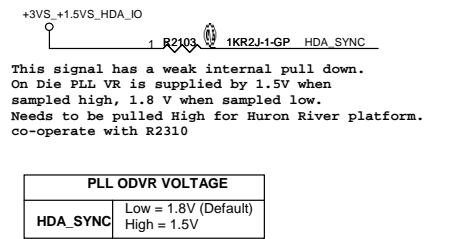
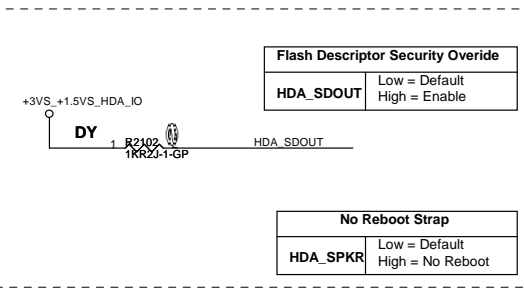
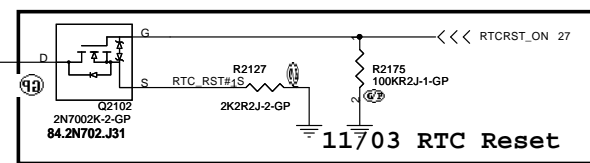
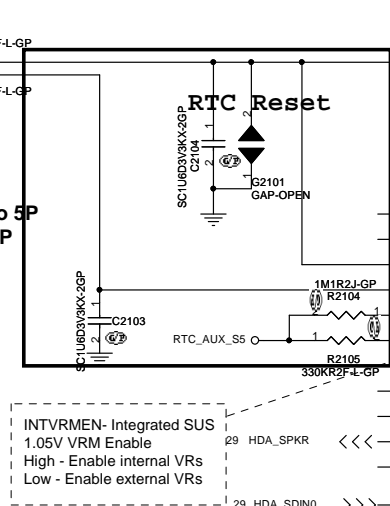
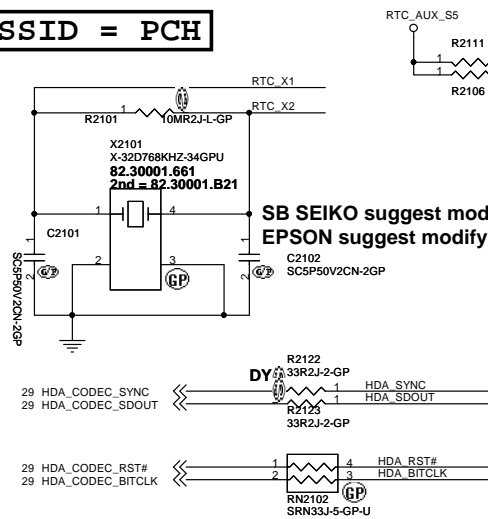
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

PCIECLKRQ1# and PCIECLKRQ2#  
Support S0 power only

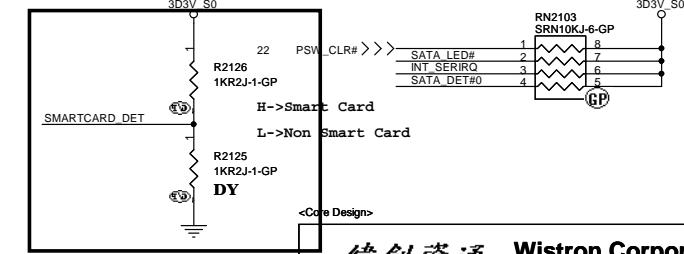
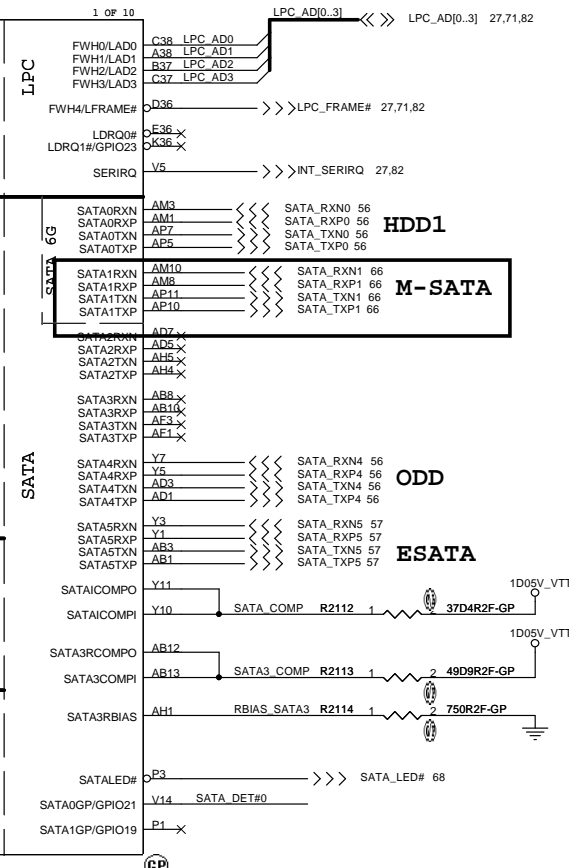
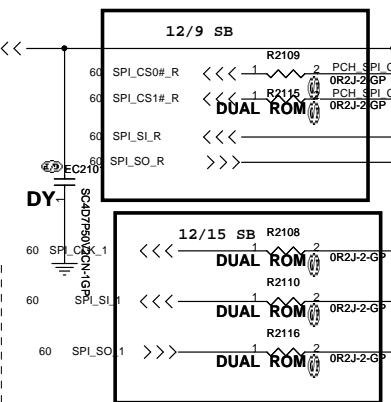
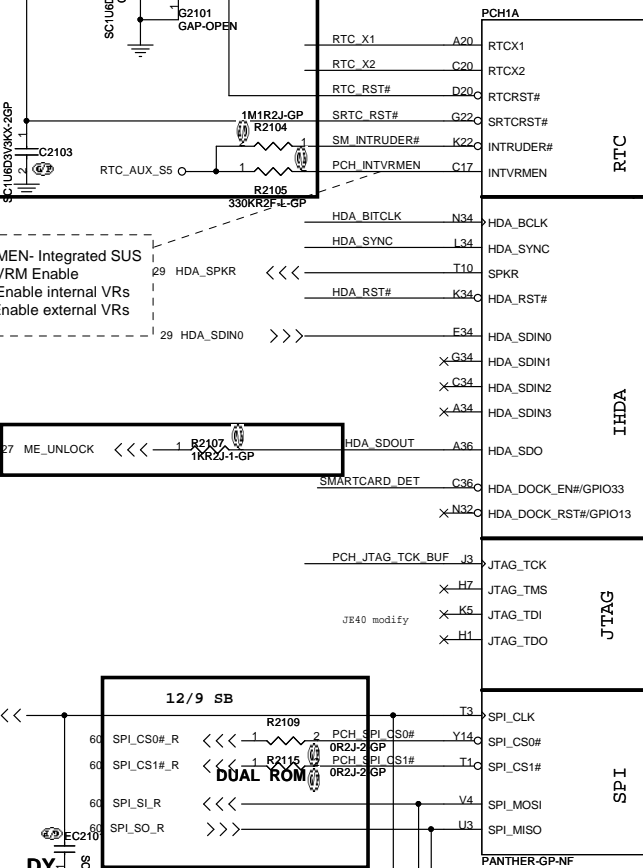
<div> <div>  <div> <b>緯創資通</b> </div> </div> <div> <div> <b>Wistron Corporation</b> </div> <div> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  Taipet Hsien 221, Taiwan, R.O.C. </div> </div> </div>			
Title			
<b>PCH (PCI-E/SMBUS/CLOCK/CL)</b>			
Size	Document Number	Rev	
Custom	<b>BD50-HC</b>	<b>-1</b>	
Date:	Thursday, March 29, 2012	Sheet	20 of 109

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SSID = PCH



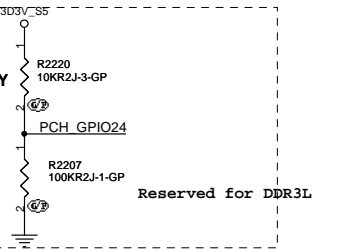
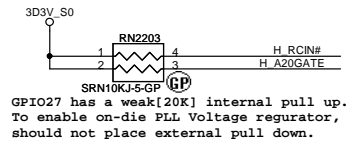
HDA\_SYNC:  
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode.  
1K external pull-up resistor is required on this signal on the board.  
Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up.  
A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.





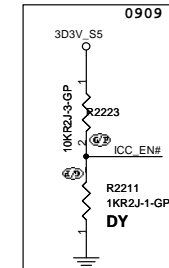
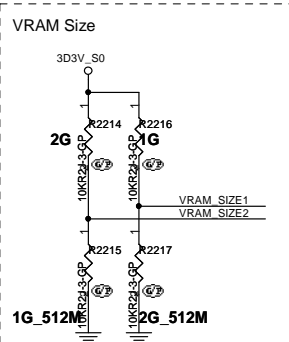
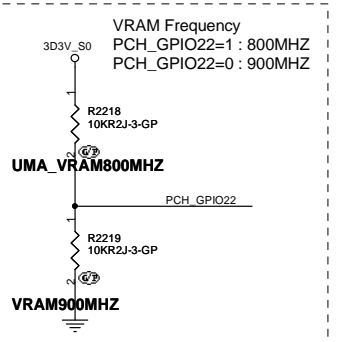
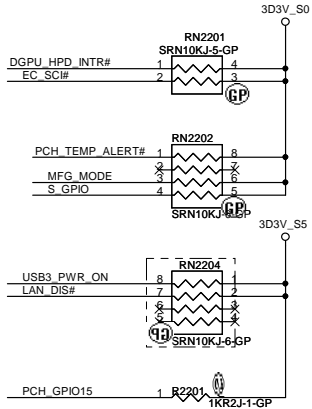
# SSID = PCH

Note:  
For PCH debug with XDP, need to NO STUFF R2218



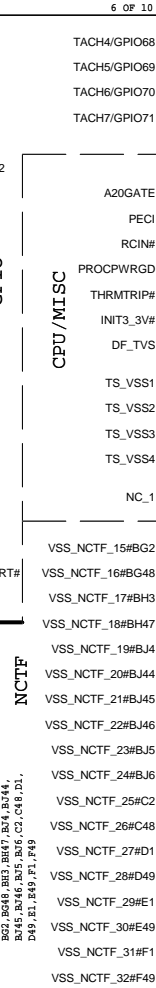
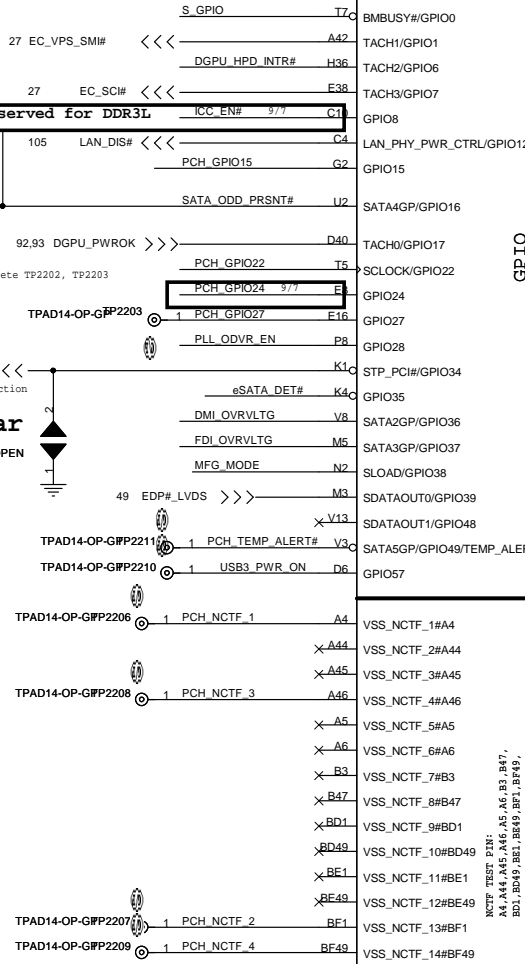
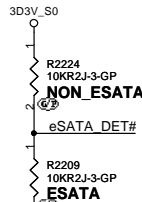
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

	H	L
EDP#_LVDS	LVDS	eDP



## PassWord Clear

G2201  
GAP-OPEN



## NCTF

NCTF TEST PIN:  
A4, A44, A46, A46, A5, A6, B3, B47,  
B1, B49, B51, B51, B51, B51, B51,  
B45, B46, B46, B46, B46, B46, B46,  
D49, E1, E49, F1, F49

TS Signal Disable Guideline:  
TS\_VSS1, TS\_VSS2, TS\_VSS3 and TS\_VSS4  
should not float on the motherboard. They should  
be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved  
via soft-strap. The default is integrated clock  
enable.

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipet Hsien 221, Taiwan, R.O.C.

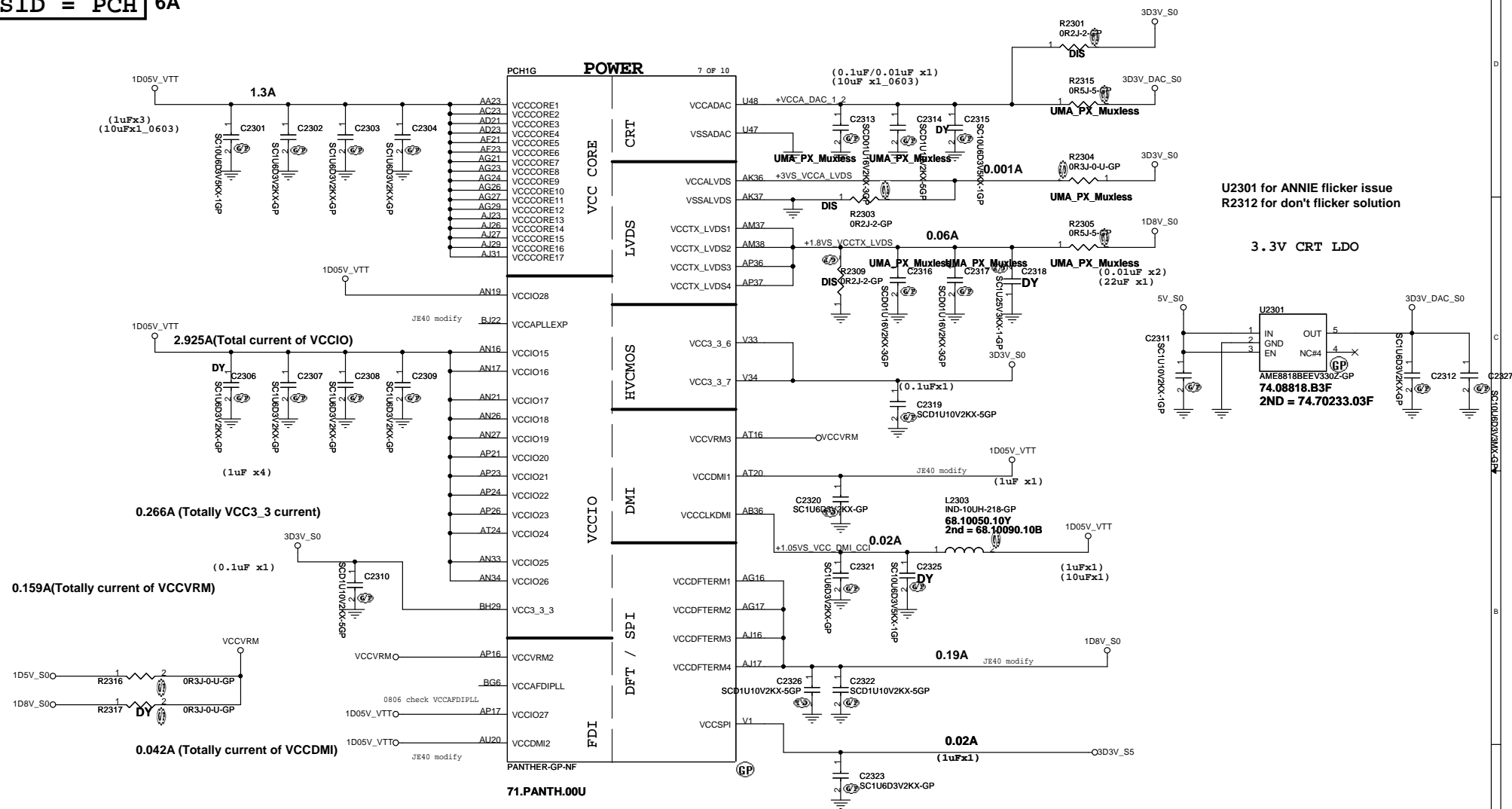
Title: **PCH (GPIO/CPU)**

Size: A3 Document Number: **BAD50-HC** Rev: **-1**

Date: Saturday, March 03, 2012 Sheet: 22 of 109



SSID = PCH 6A



&lt;Core Design&gt;

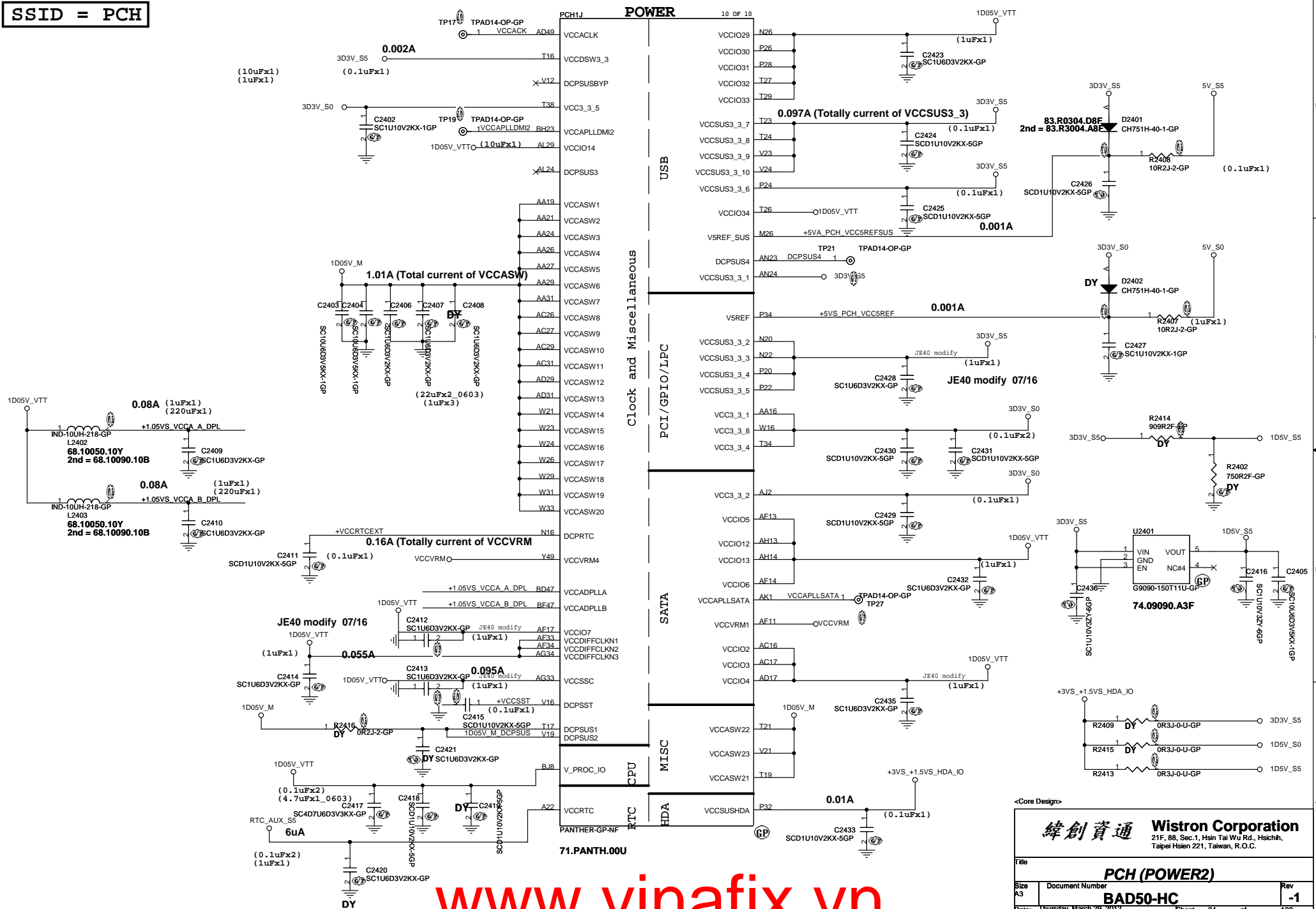
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title	<b>PCH (POWER1)</b>
-------	---------------------

Size A3	Document Number <b>BAD50-HC</b>	Rev <b>-1</b>
Date: Thursday, March 29, 2012	Sheet 23 of 109	

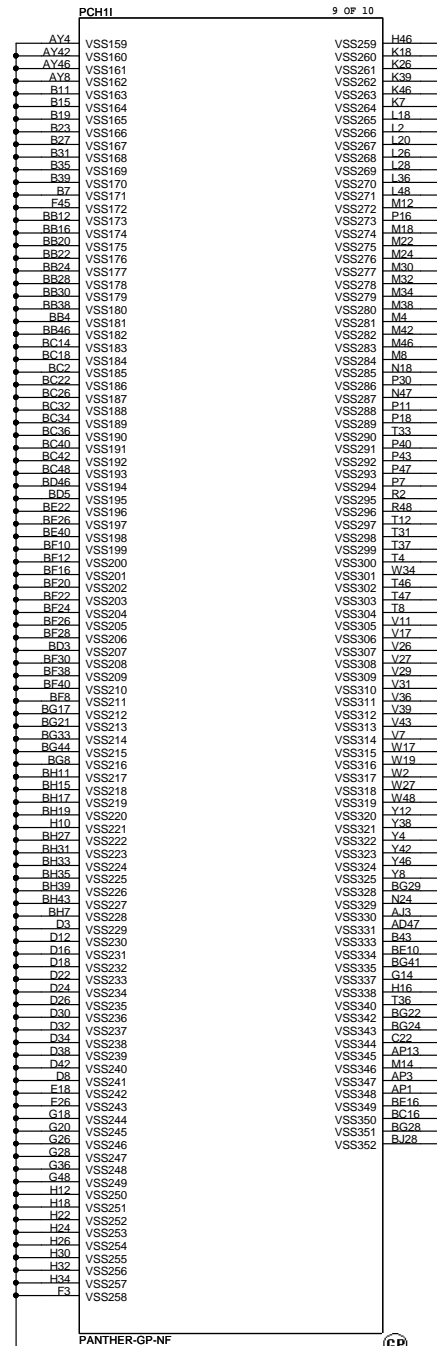
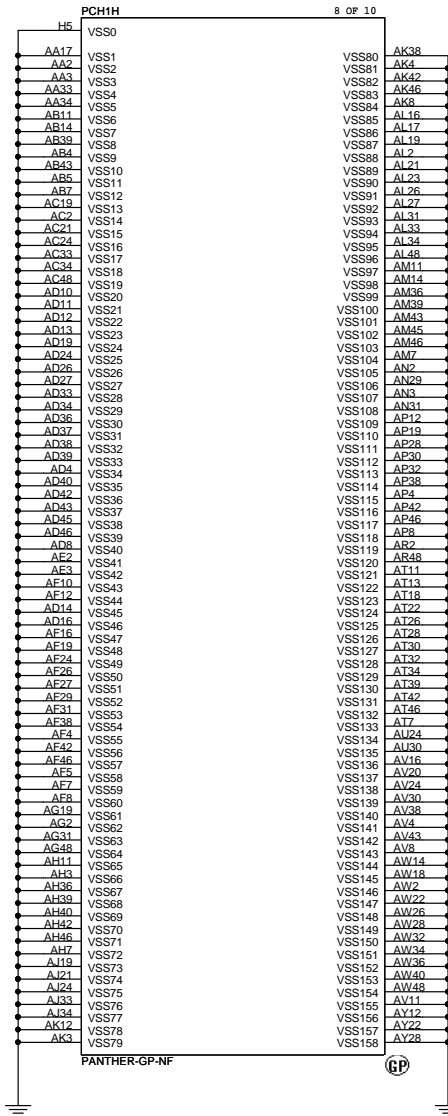
[www.vinafix.vn](http://www.vinafix.vn)

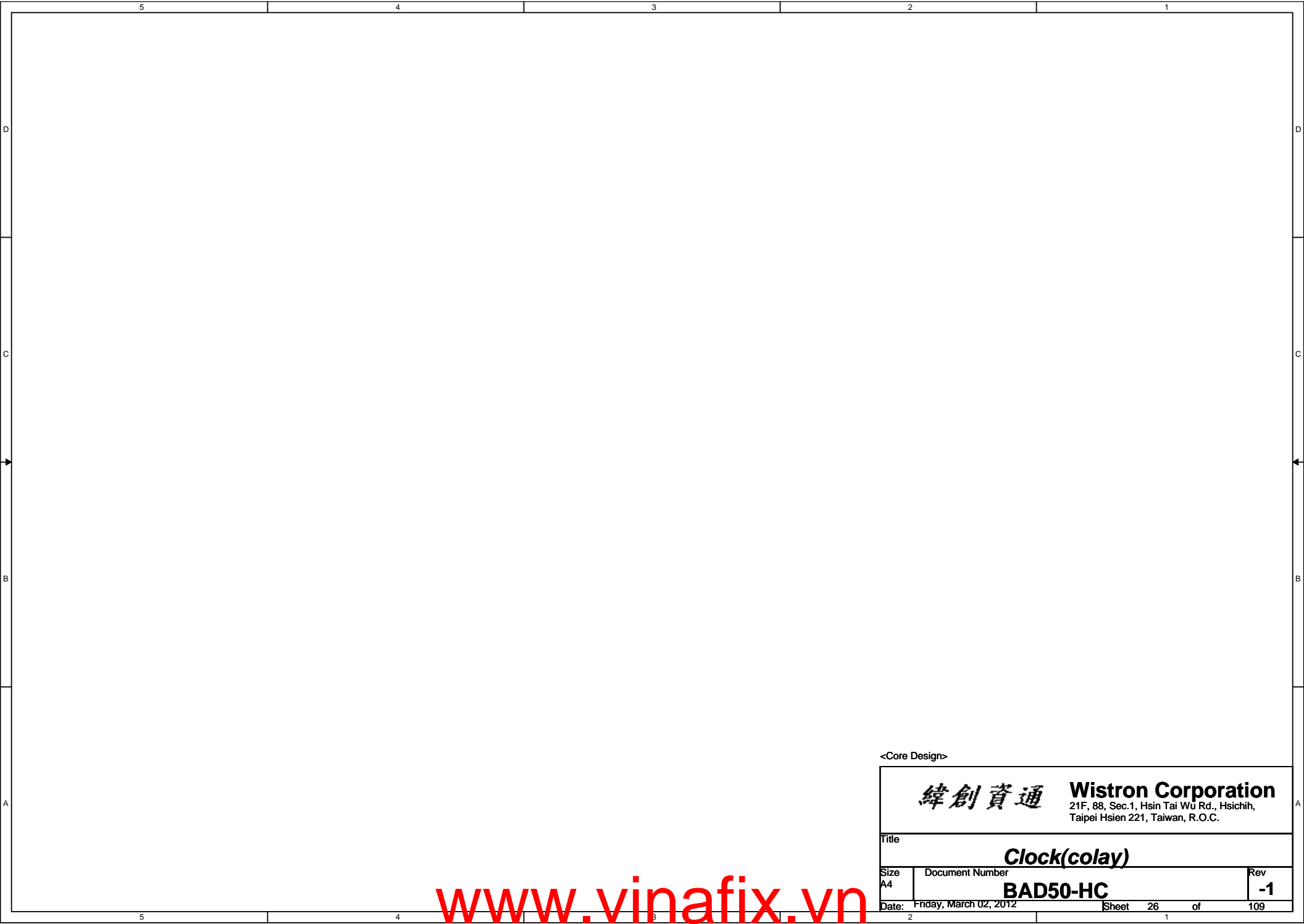
SSID = PCH



<div> <div>  <div> <b>緯創資通</b>  <b>Wistron Corporation</b>            21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,            Taipei Hsien 221, Taiwan, R.O.C.         </div> </div> </div>			
Title			
<div> <div> <b>PCH (POWER2)</b>  <b>BAID50-HC</b> </div> <div>Rev -1</div> </div>			
Size A3	Document Number		
Date:	Thursday, March 29, 2012	Sheet 24 of	109

SSID = PCH



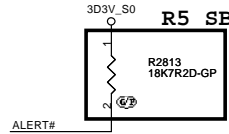
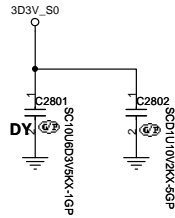


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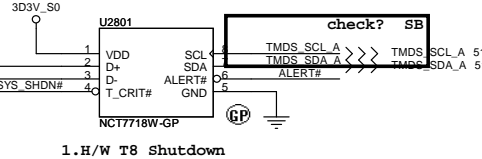
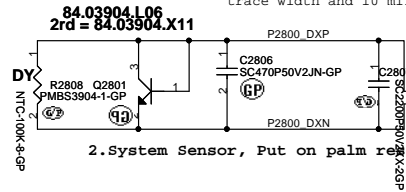
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
Clock(colay)		
Size	Document Number	Rev
A4	BAD50-HC	-1
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SSID = Thermal



Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.



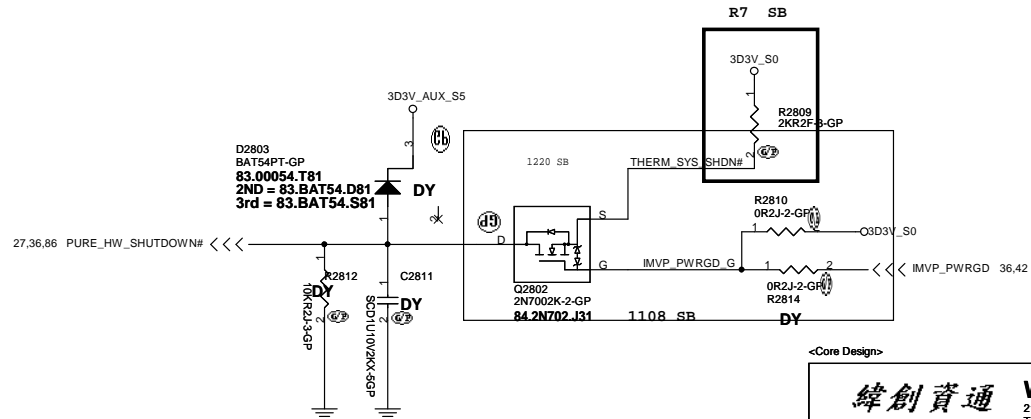
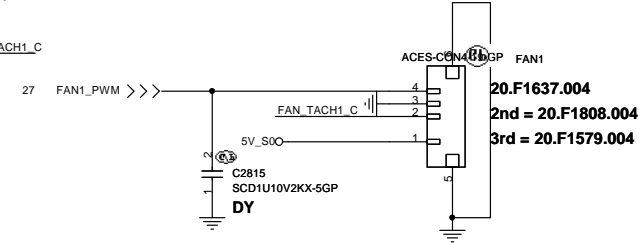
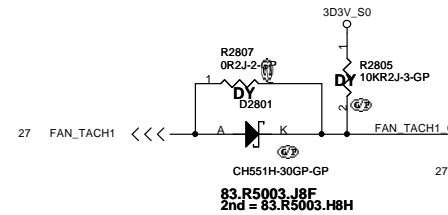
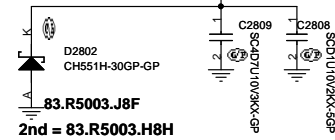
ALERT# /T CRIT#  
Pull-up Resistor

R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	87°C	97°C	107°C	117°C	
79°C	89°C	99°C	109°C	119°C	
81°C	91°C	101°C	111°C	121°C	
83°C	93°C	103°C	113°C	123°C	
85°C	95°C	105°C	115°C	125°C	

T\_CRIT temperature strapping point

Fan controller P2793

\*Layout\* 15 mil







# AUDIO OP AMPLIFIER

JE40 delete AMP function

<Core Design>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Audio AMP**

Size  
A4

Document Number

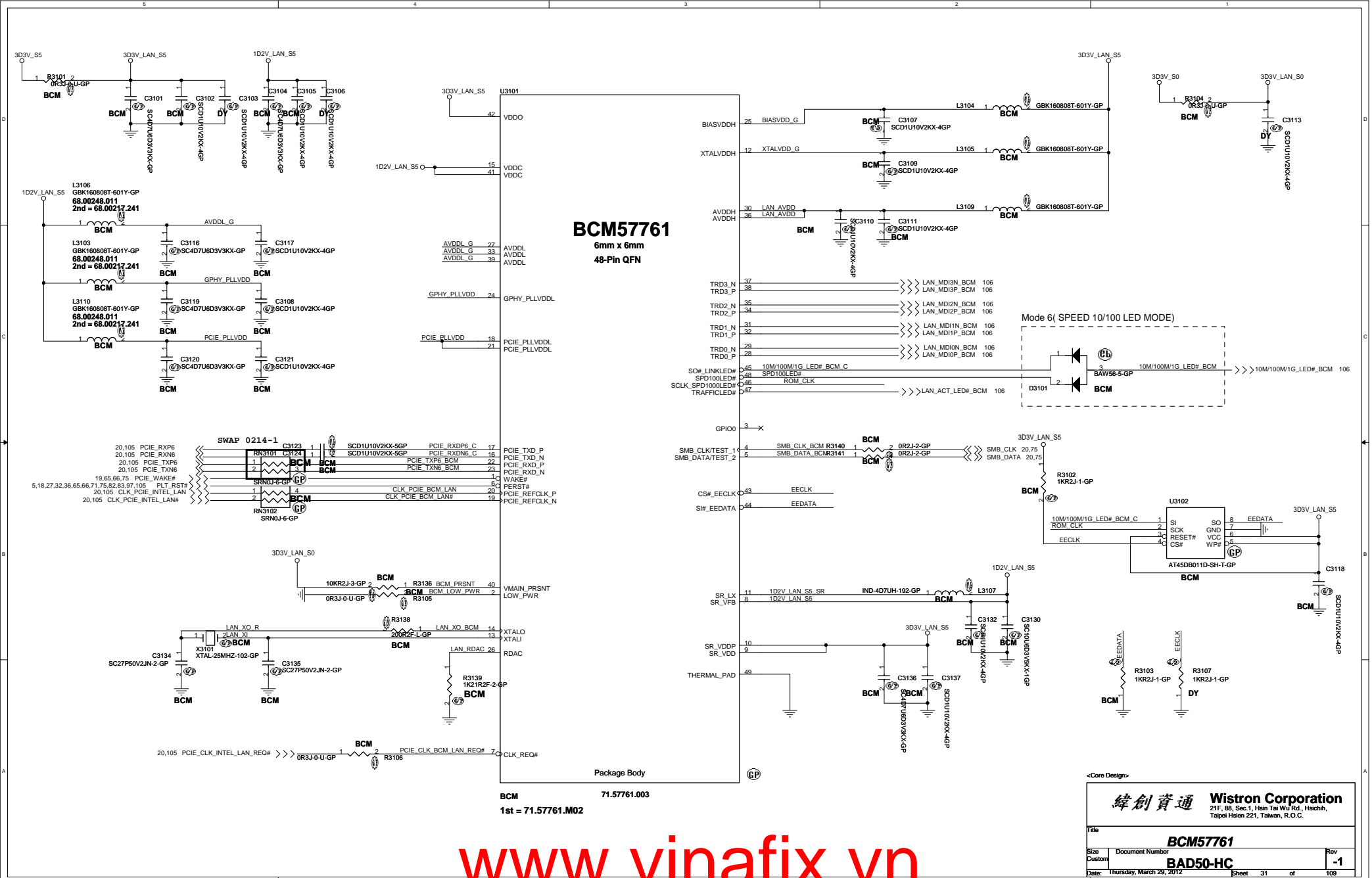
**BAD50-HC**

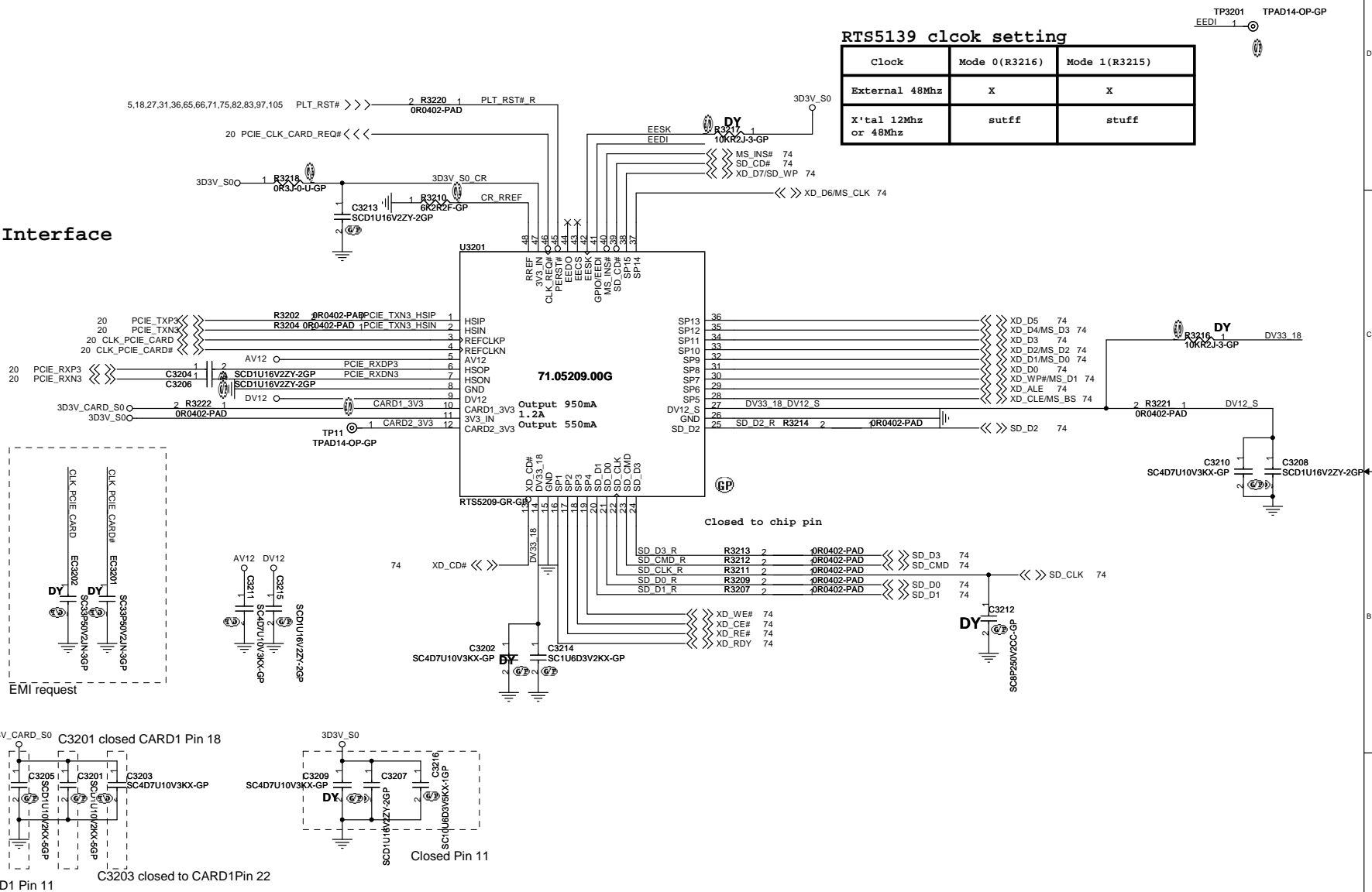
Rev

**-1**

Date: Friday, March 02, 2012

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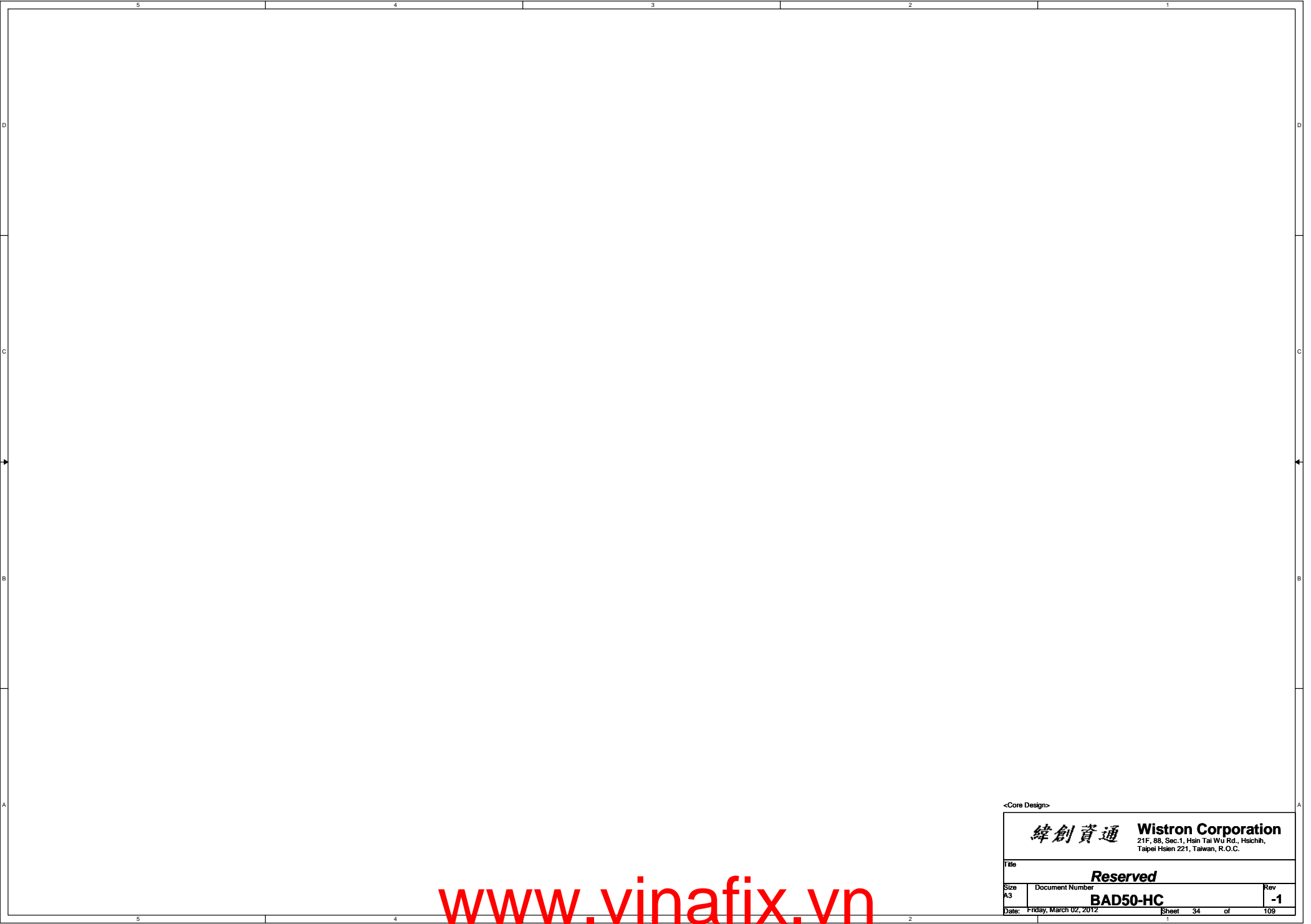




( Blanking )

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number  BAD50-HC		Rev  -1
Date:	Friday, March 02, 2012	Sheet 33 of	109



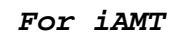
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緯創資通		Wistron Corporation	
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Title			
Reserved			
Size	Document Number		Rev
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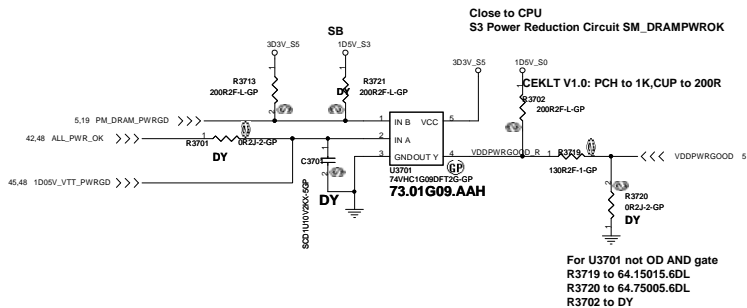
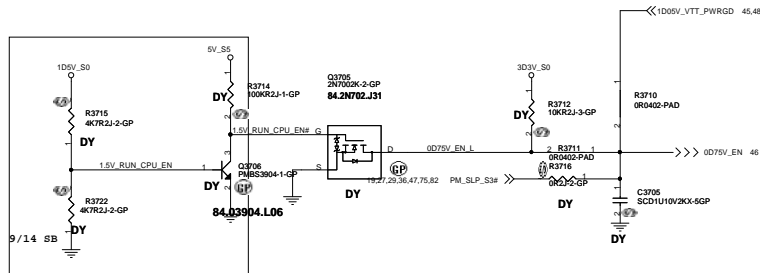
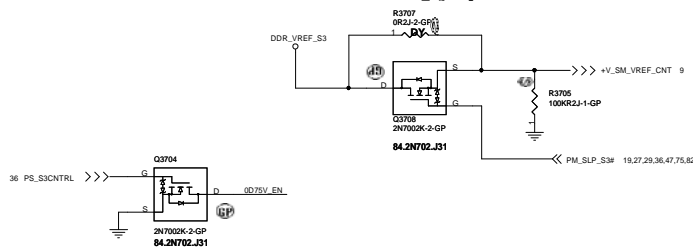
reserve

[www.vinafix.vn](http://www.vinafix.vn)

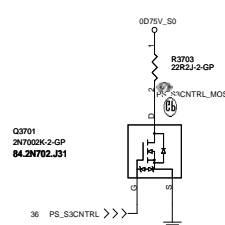




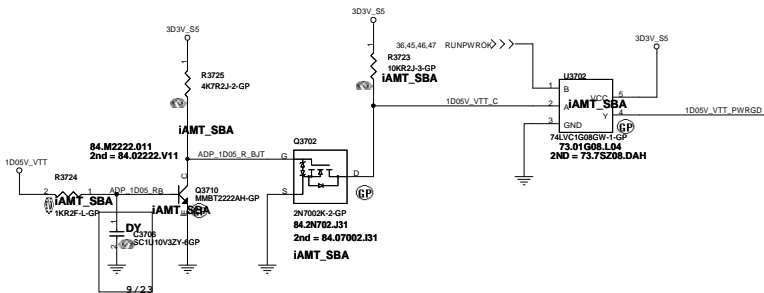
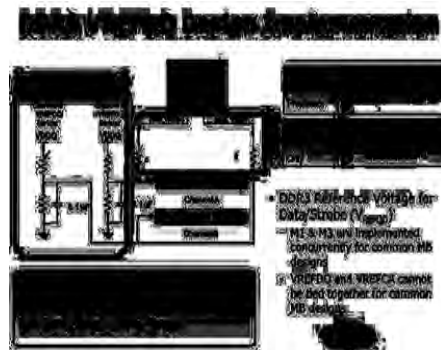
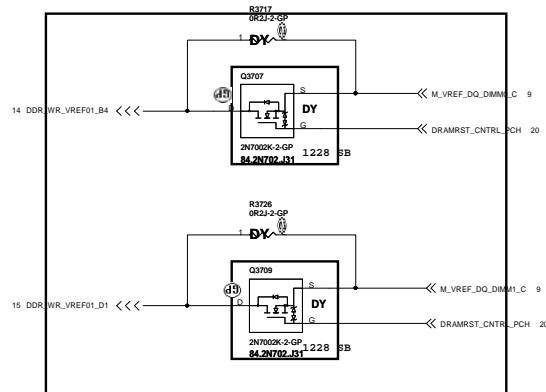
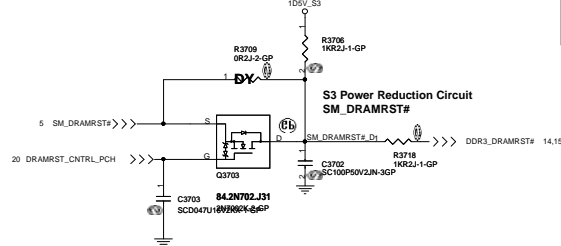
Close to CPU  
S3 Power Reduction Circuit Processor VREF\_DQ Implementation



Close to DIMM  
S3 Power Reduction Circuit SM\_DRAMPWROK

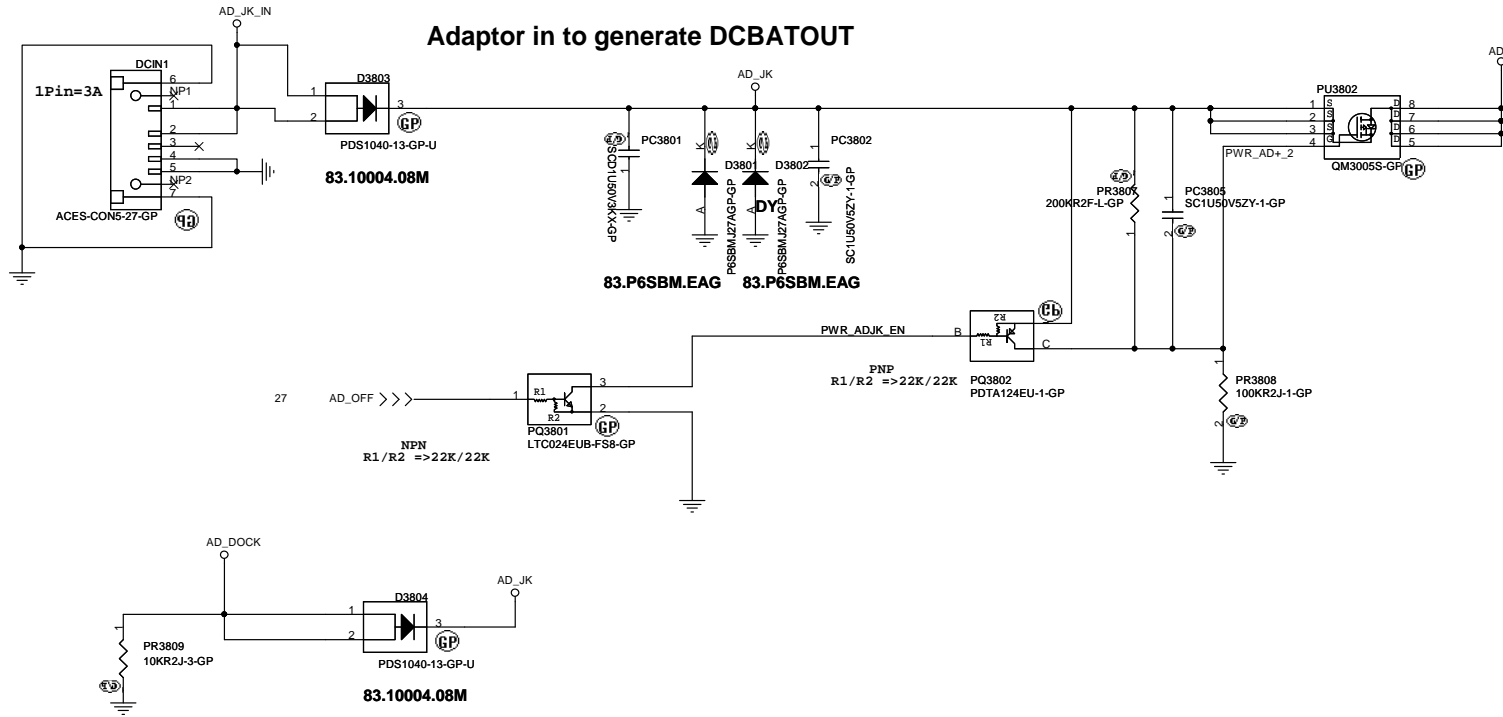


Close to CPU  
S3 Power Reduction Circuit SM\_DRAMPWROK



<Core Design>

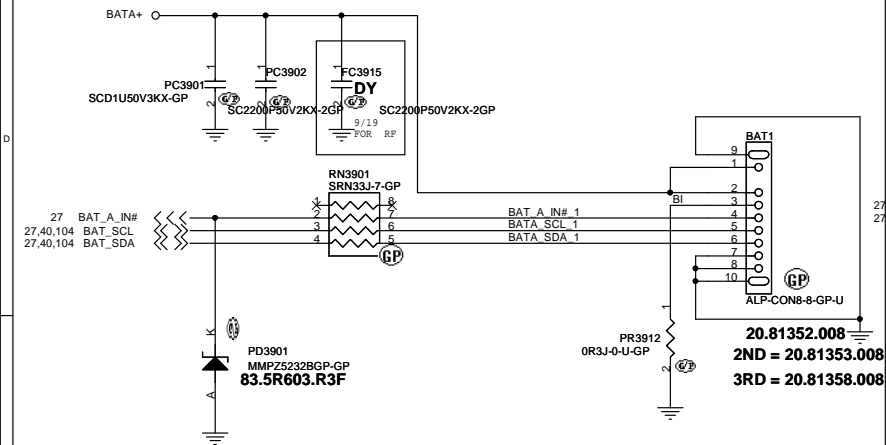
## Adaptor in to generate DCBATOUT



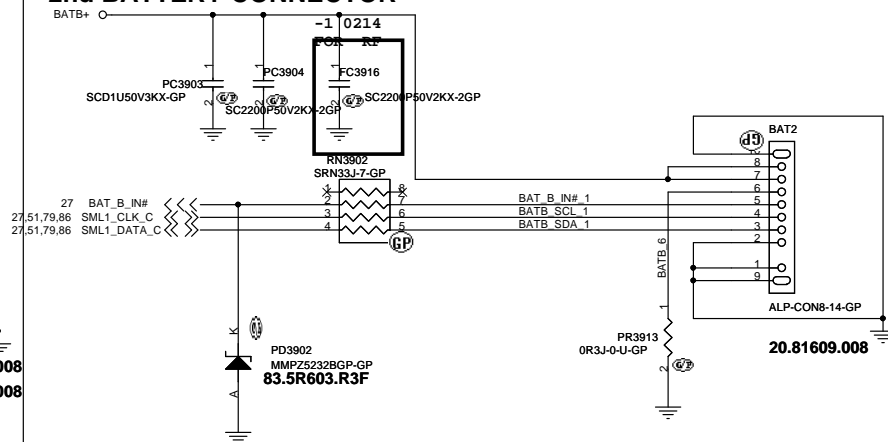
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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>DCIN JACK</b>	
Size A3	Document Number <b>BAD50-HC</b>
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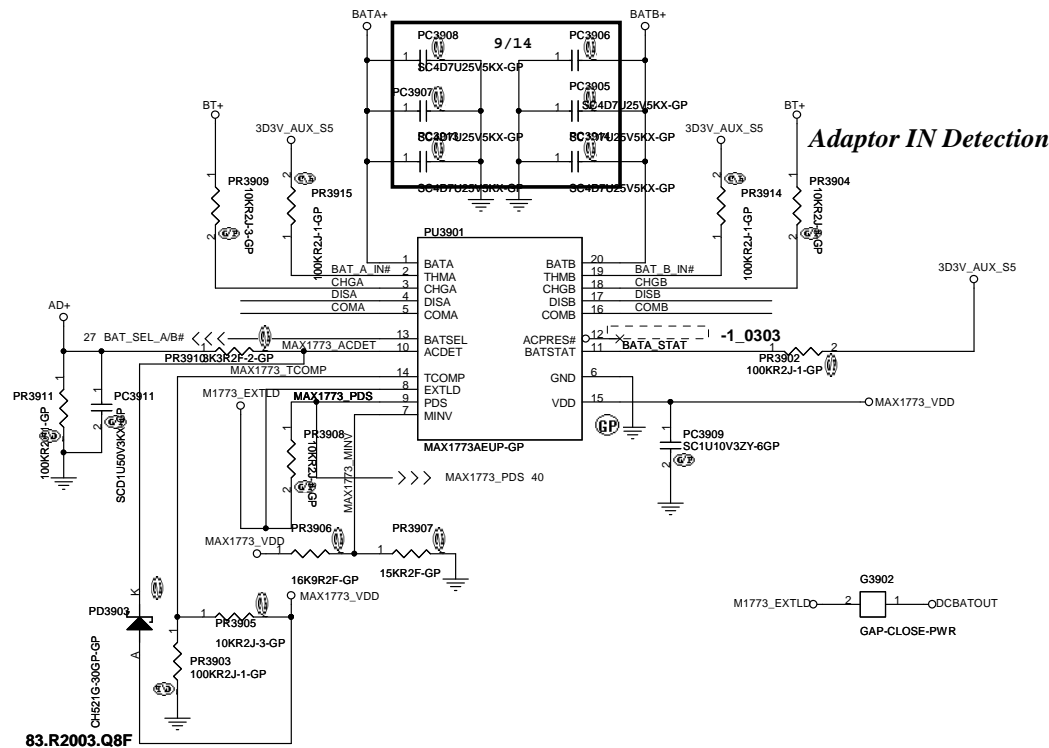
## MAIN BATTERY CONNECTOR



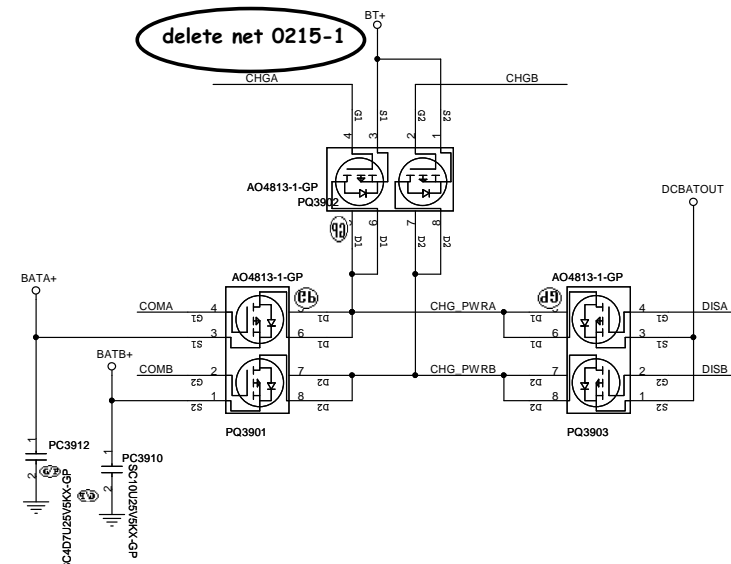
## 2nd BATTERY CONNECTOR



## BATTERY SWITCH



delete net 0215-1



SSID = Charger

A8( ANNIE/ASTRO)  
PR4014, PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

change to 74.24727 073

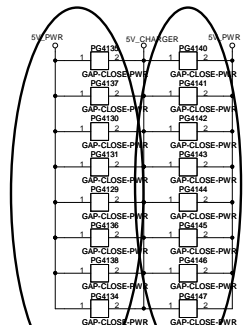
delete net

<Core Design>

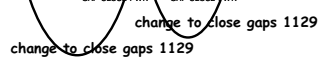
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File CHARGER BQ24727  
Size Custom Document Number BAD50-HC Rev -1  
Date: Thursday, March 29, 2012 Sheet 40 of 109

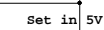
www.vinafix.vn

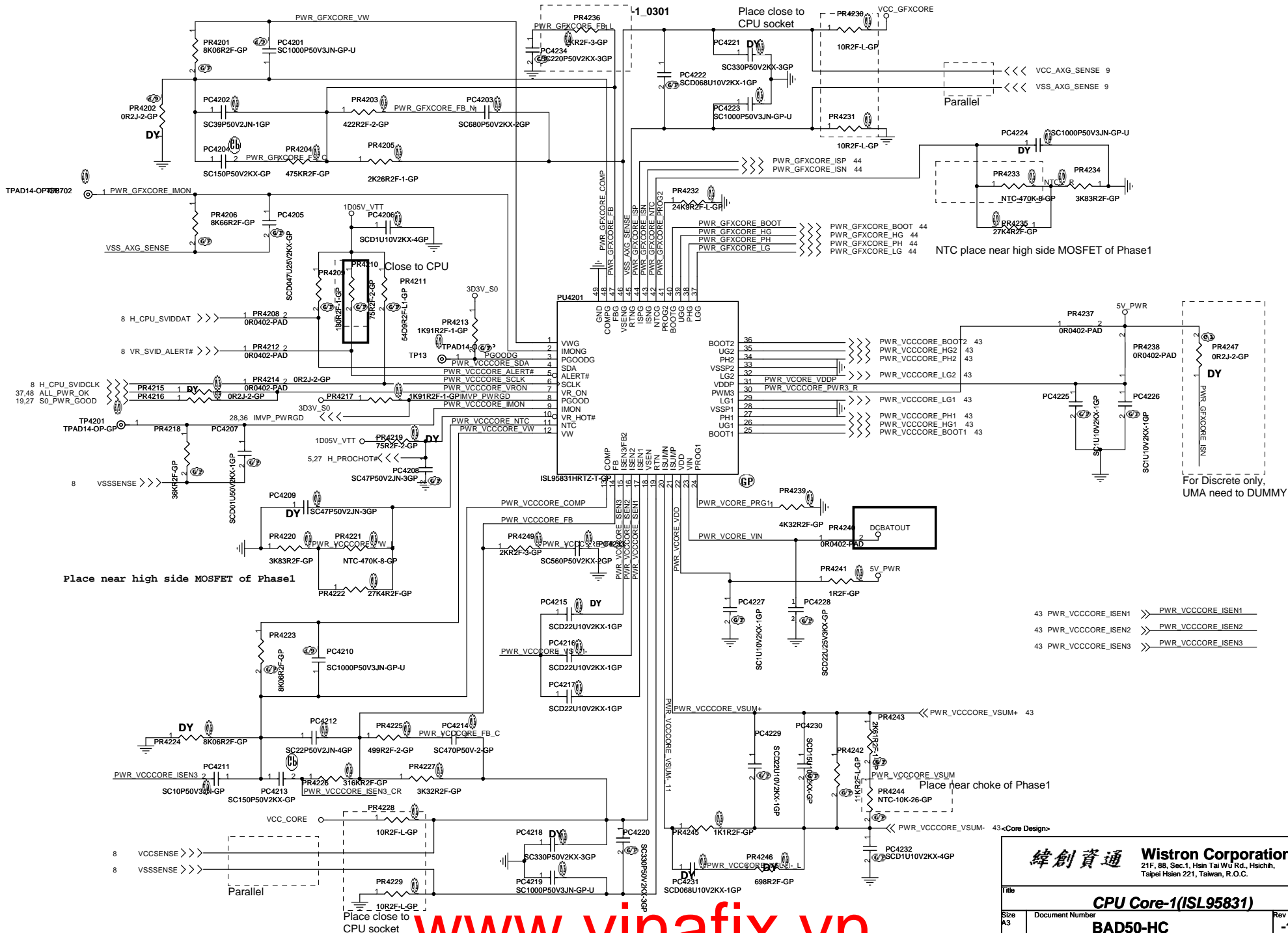


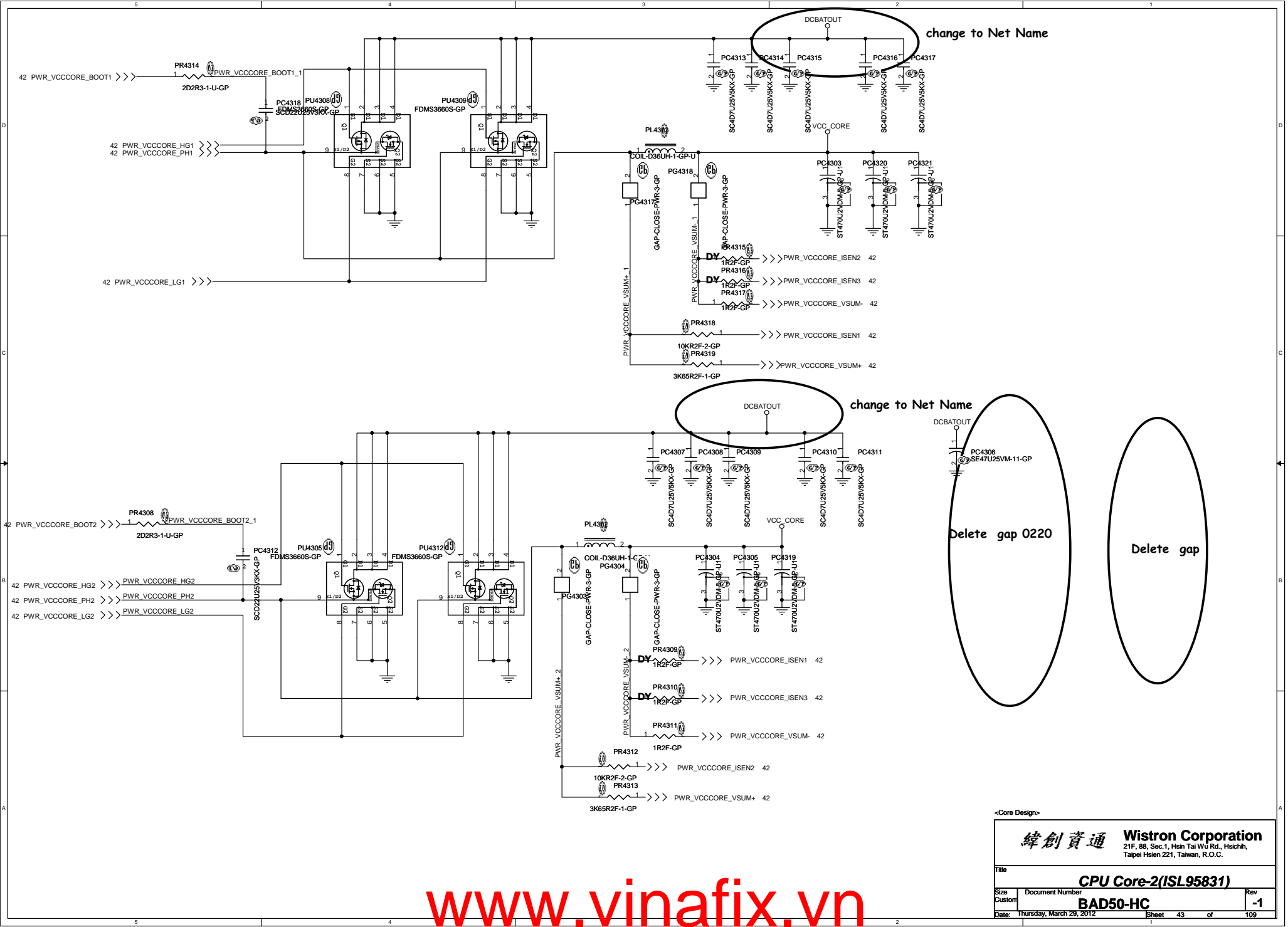
OCP setting  
change to 130K  
Set in 9.5652A



Iomax=15A  
OCP>21A


$$V_{out} = 2 * ( 1 + PR4113 / PR4117 )$$

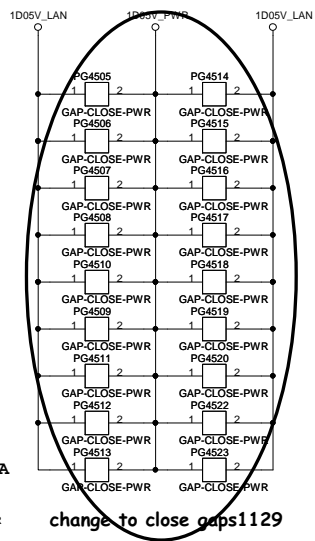
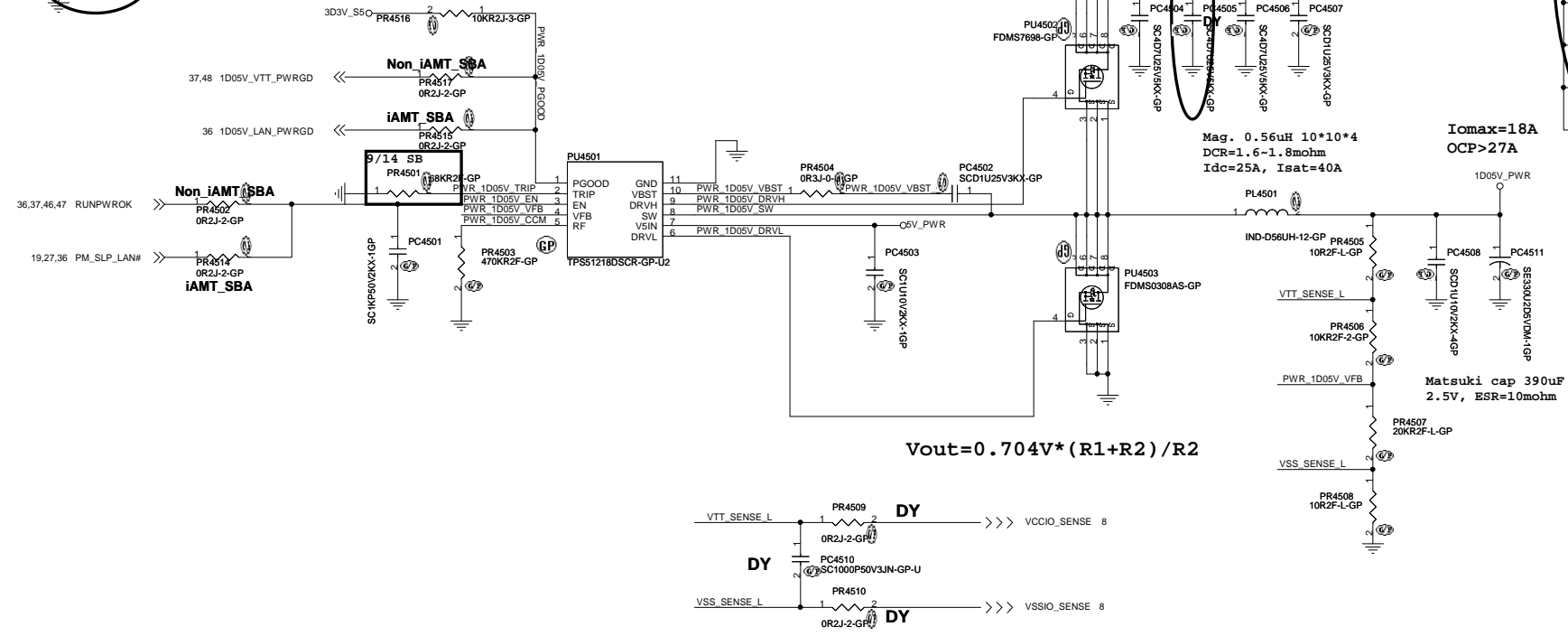




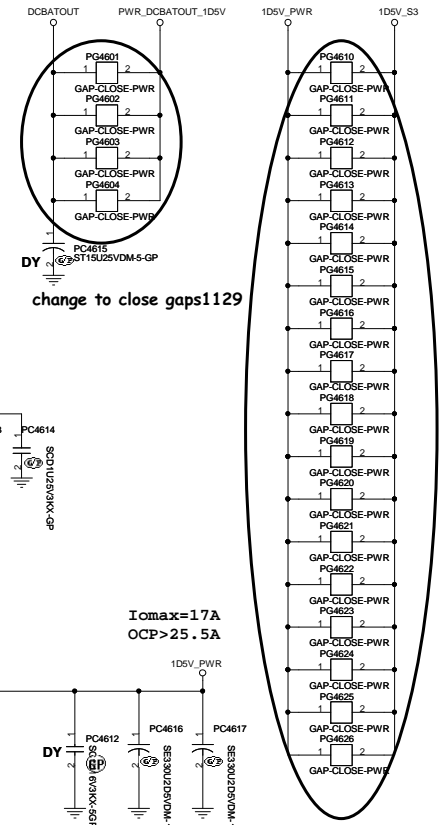




## TPS51218 for 1D05V

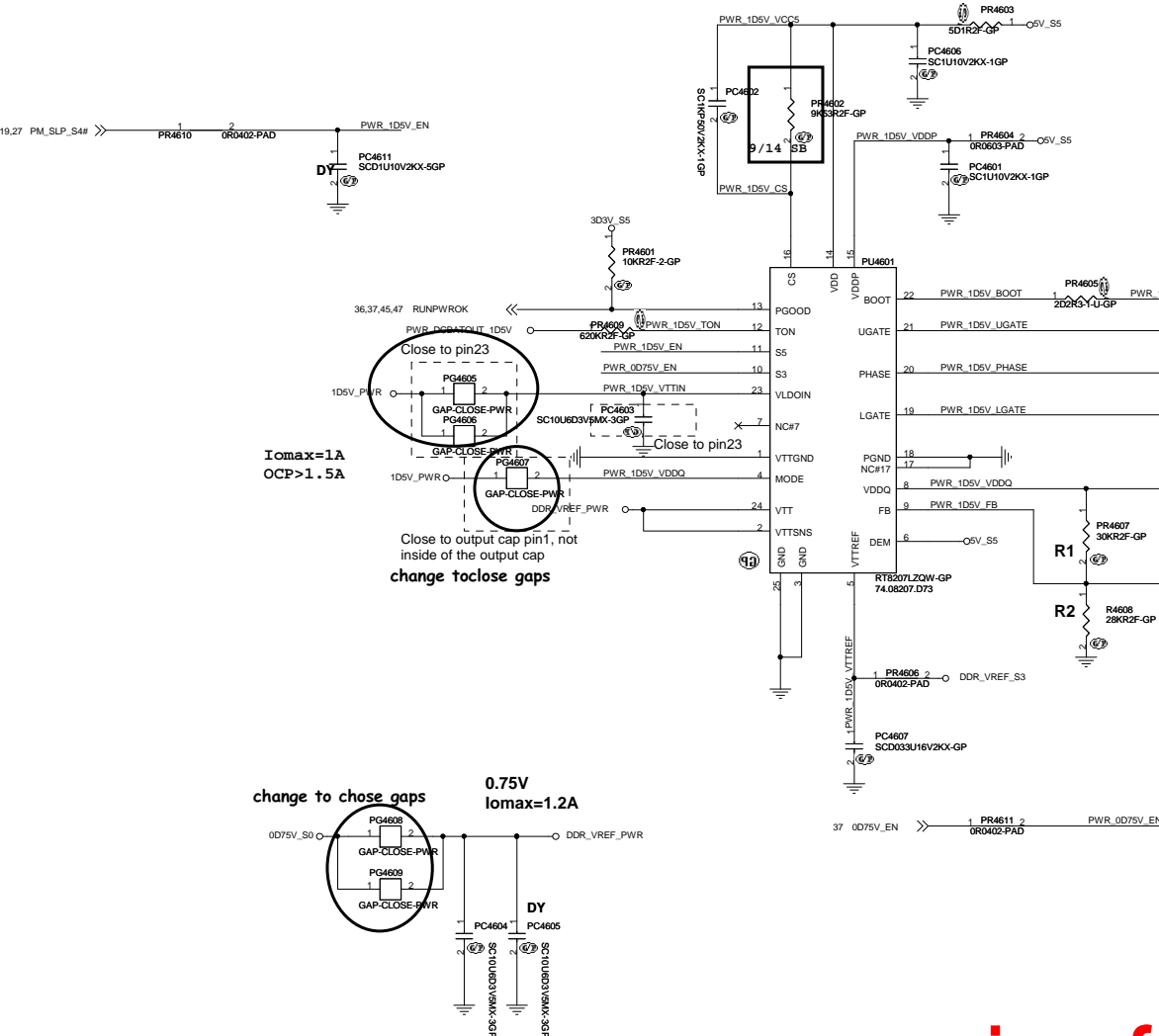


## RT8207L for 1D5V



change to close gaps1129

Iomax=17A  
OCP>25.5A

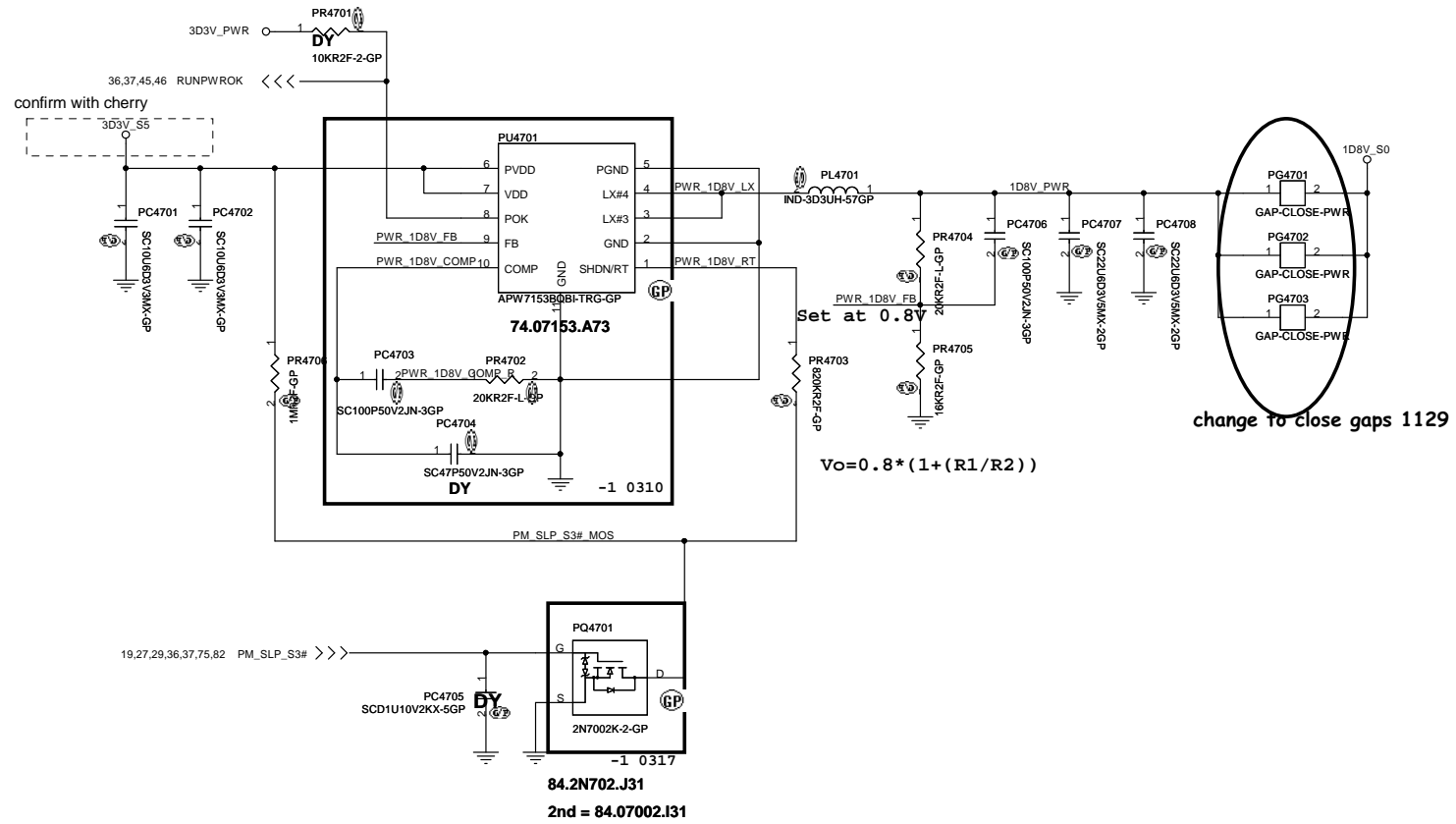
$$V_{out} = 0.75 * (1 + R_1/R_2)$$
$$V_{out} = 0.75 * (1 + 30K/30K) = 1.5V$$


<Core Design>

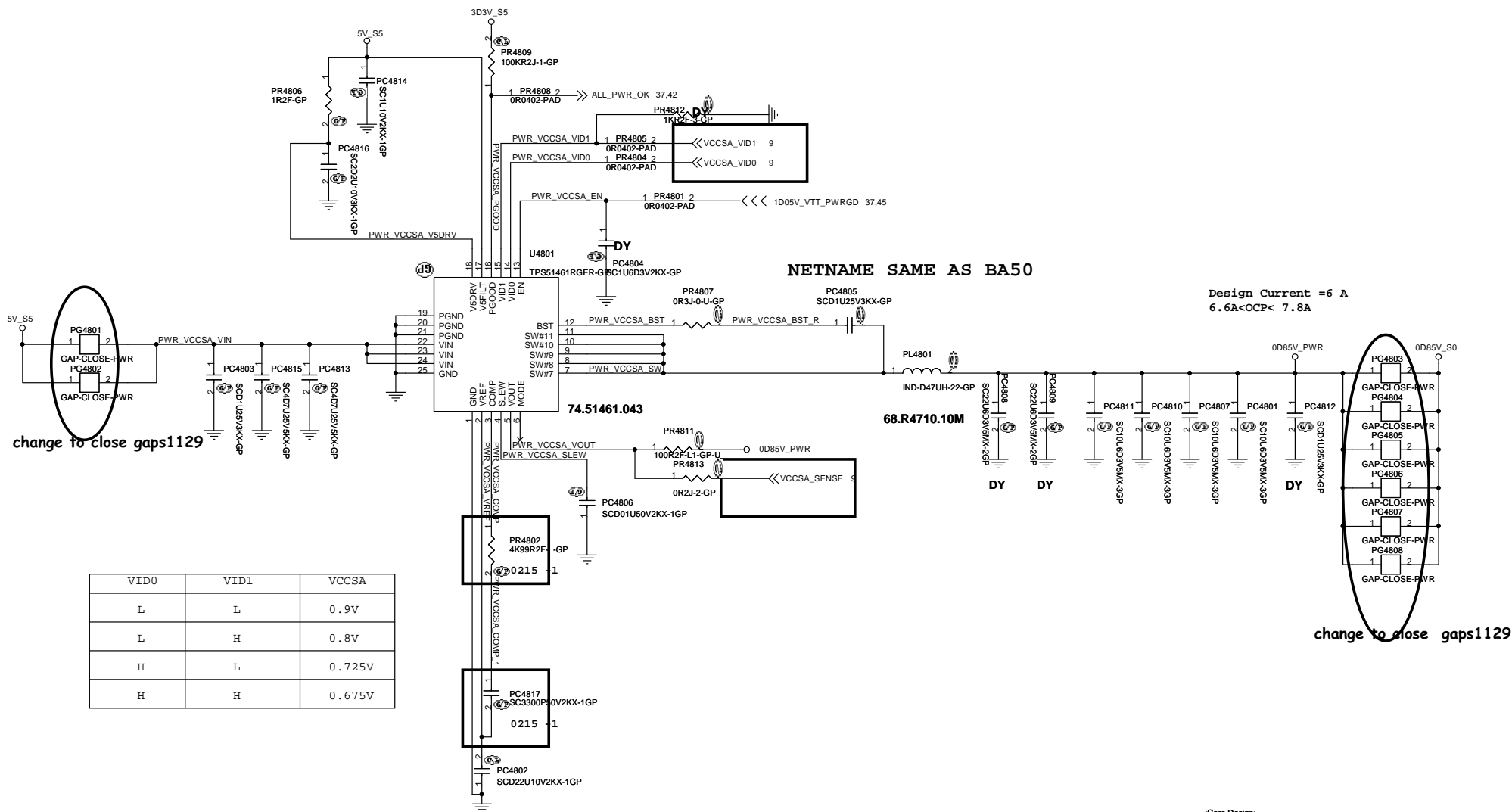
**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>RT8207L</b>			
Size Custom	Document Number		Rev
	<b>BAD50-HC</b>		<b>-1</b>
Dealer	Thursday, March 29, 2012	Sheet 46 of	109

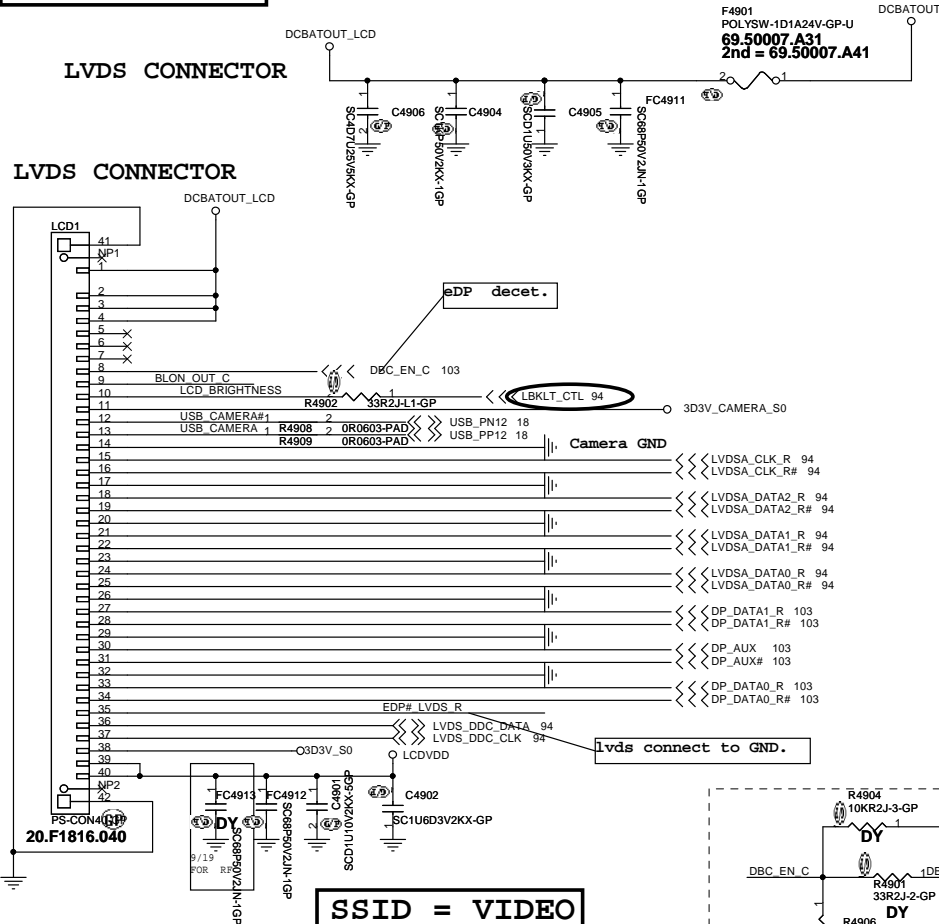
# APW7153B for 1D8V\_S0



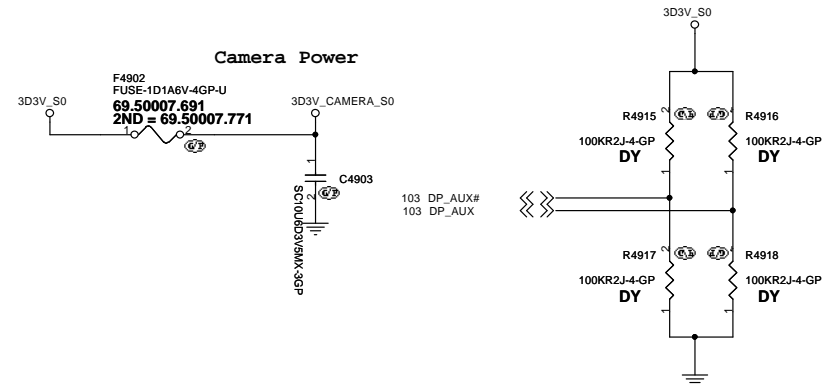
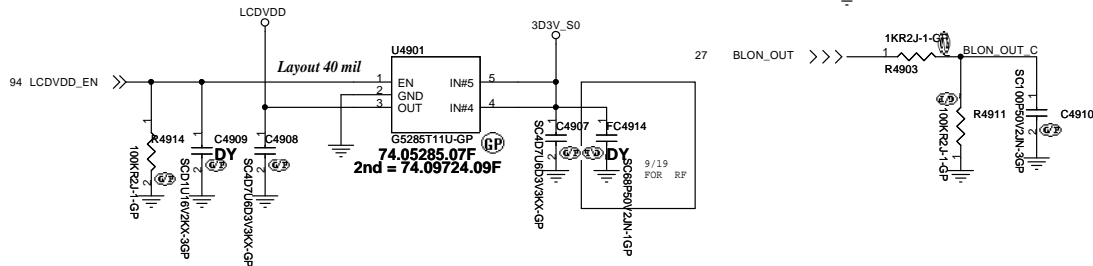
# TPS51461 for VCCSA



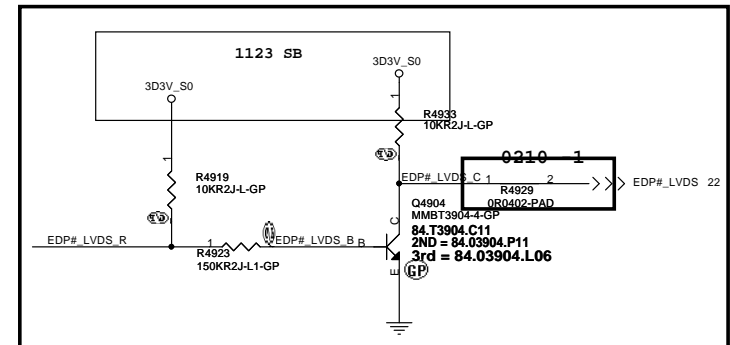
## INVERTER POWER



LCD POWER for ANNIE



Note: Place pull up resistor within 2 inch of CPU



LVDS0_CLK#	DY	1	FC4901
LVDS0_CLK#_R	DY	1	1SC4D7P50V2CN-1GP 1 FC4902
LVDS0_DATA2_R	DY	1	1SC4D7P50V2CN-1GP FC4903
LVDS0_DATA2_R#	DY	1	1SC4D7P50V2CN-1GP 1 FC4904
LVDS0_DATA1_R	DY	1	1SC4D7P50V2CN-1GP FC4905
LVDS0_DATA1_R#	DY	1	1SC4D7P50V2CN-1GP 1 FC4906
LVDS0_DATA0_R	DY	1	1SC4D7P50V2CN-1GP FC4907
LVDS0_DATA0_R#	DY	1	1SC4D7P50V2CN-1GP 1 FC4908
LVDS_DDC_DATA	DY	1	1SC4D7P50V2CN-1GP FC4909
LVDS_DDC_CLK	DY	1	1SC4D7P50V2CN-1GP 1 FC4910
	DY	1	1SC4D7P50V2CN-1GP

### <Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>LCD Connector</b>			
Size A3	Document Number	Rev	
	<b>BAD50-HC</b>	<b>-1</b>	
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2





( Blanking )

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
S-VIDEO			
Size	Document Number		Rev
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( Blanking )

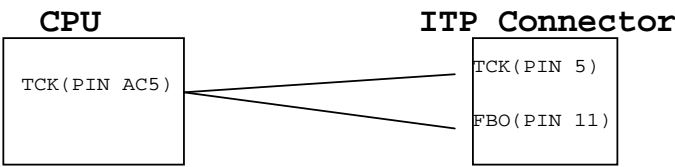
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number  BAD50-HC		Rev  -1
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SSID = User.Interface

# ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.

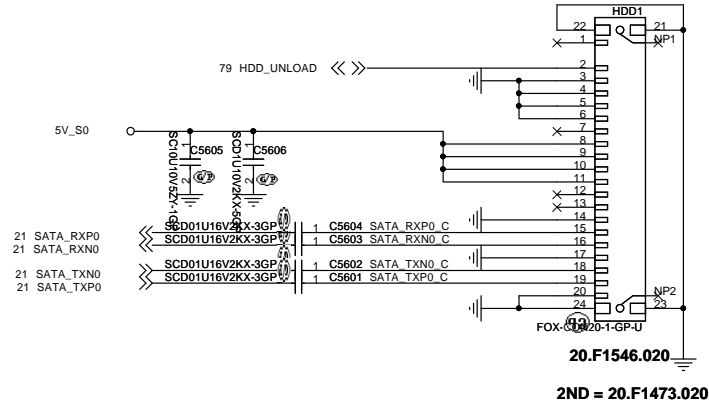


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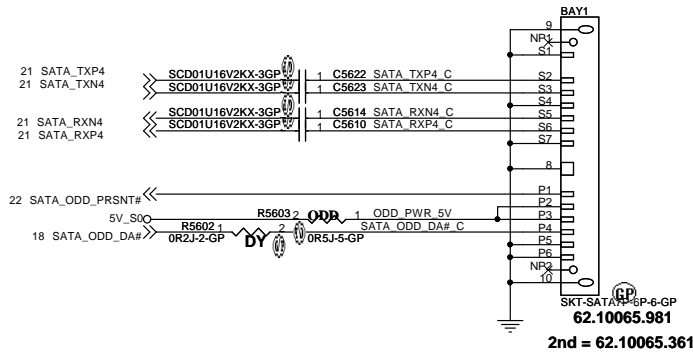
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP			
Size	Document Number		Rev
A4	BAD50-HC		-1
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SSID = SATA

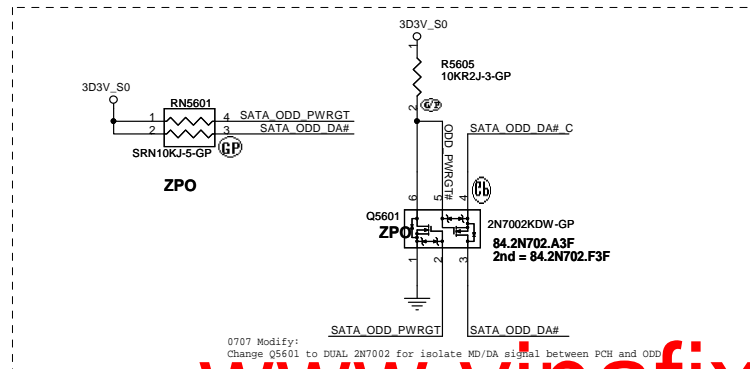
# SATA HDD Connector



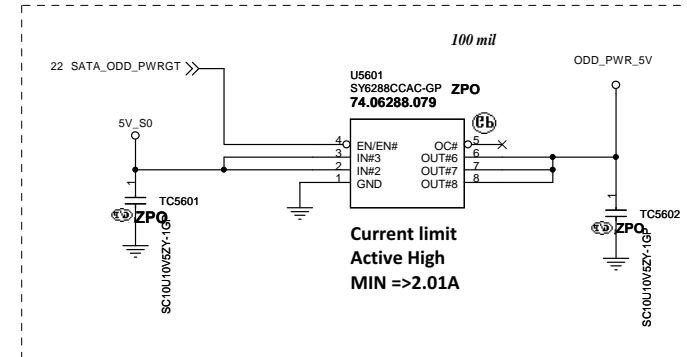
## ODD Connector 2nd source 62.10065.541 and 62.10065.A11.



SATA Zero Power ODD



SATA Zero Power ODD



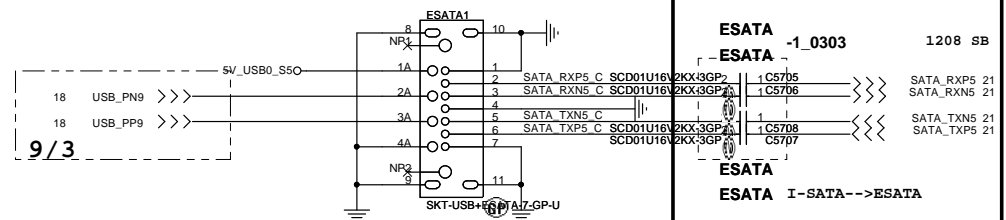
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<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title</p> <p><b>HDD/ODD</b></p>		
Size	Document Number	Rev
A3	<b>BAD50-HC</b>	-1
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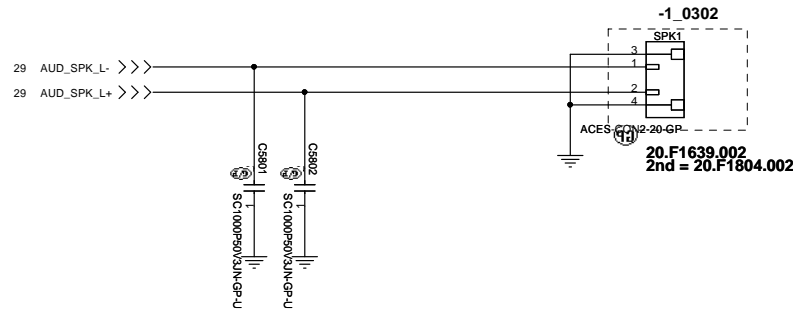
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1208 SB

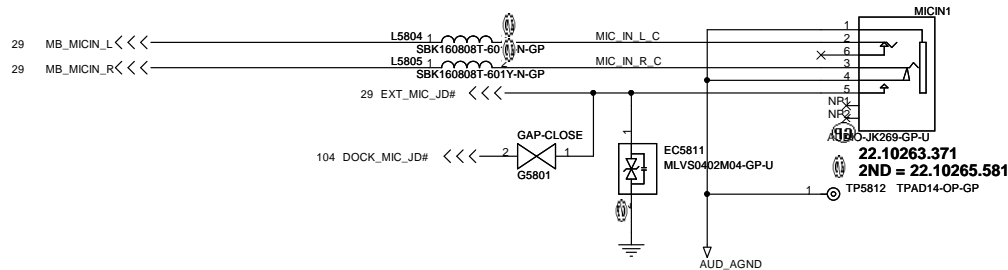


**SSID = AUDIO**

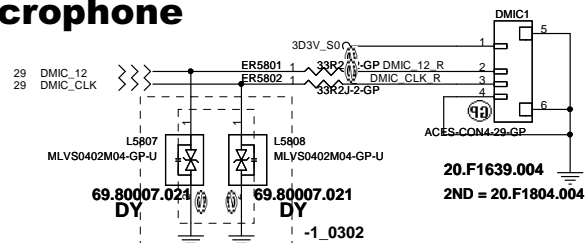
## Speaker Connector



**MIC IN**

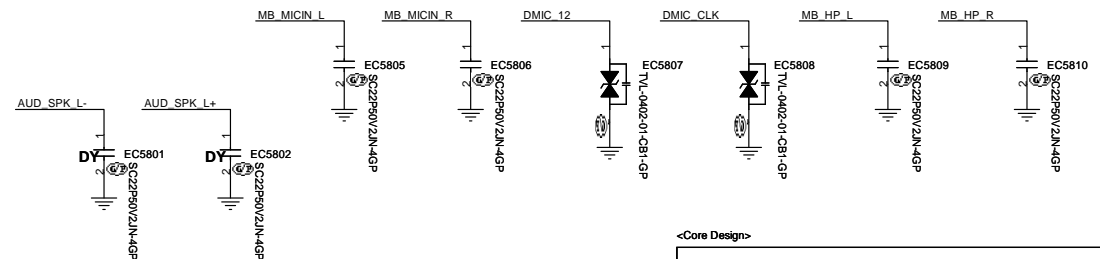
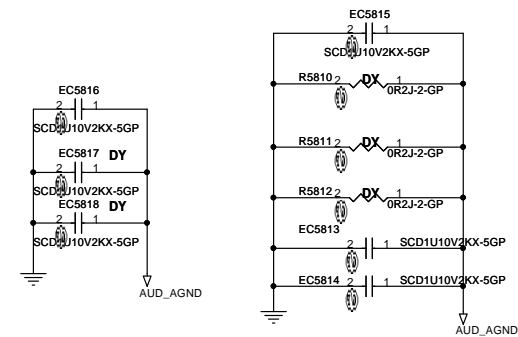
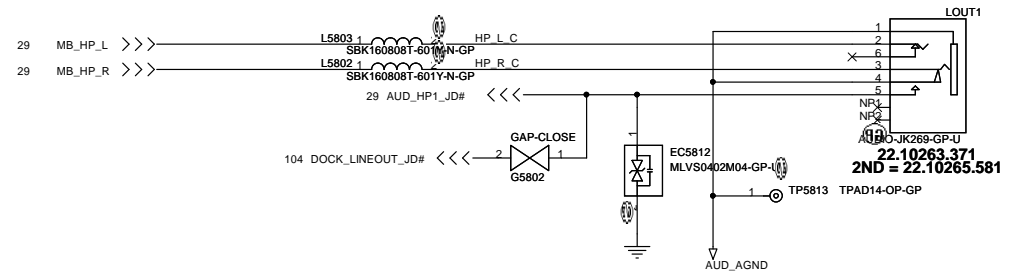


## Internal Microphone



(Varistor)  
Need confirm with EMI :  
69.80007.021 or 69.80024.011 ?

## LINE OUT



### <Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

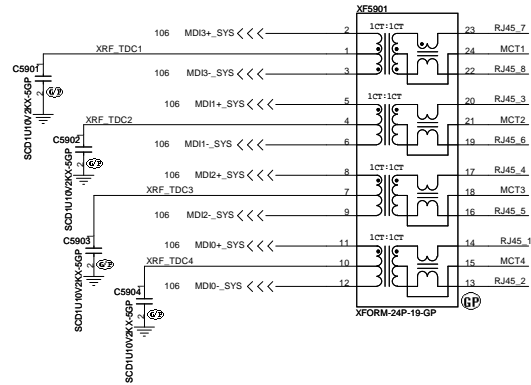
Title			
<b>Audio Jack</b>			
Size A3	Document Number		Rev
	<b>BAD50-HC</b>		<b>-1</b>
Date:	Saturday, March 03, 2012	Sheet 58 of	109

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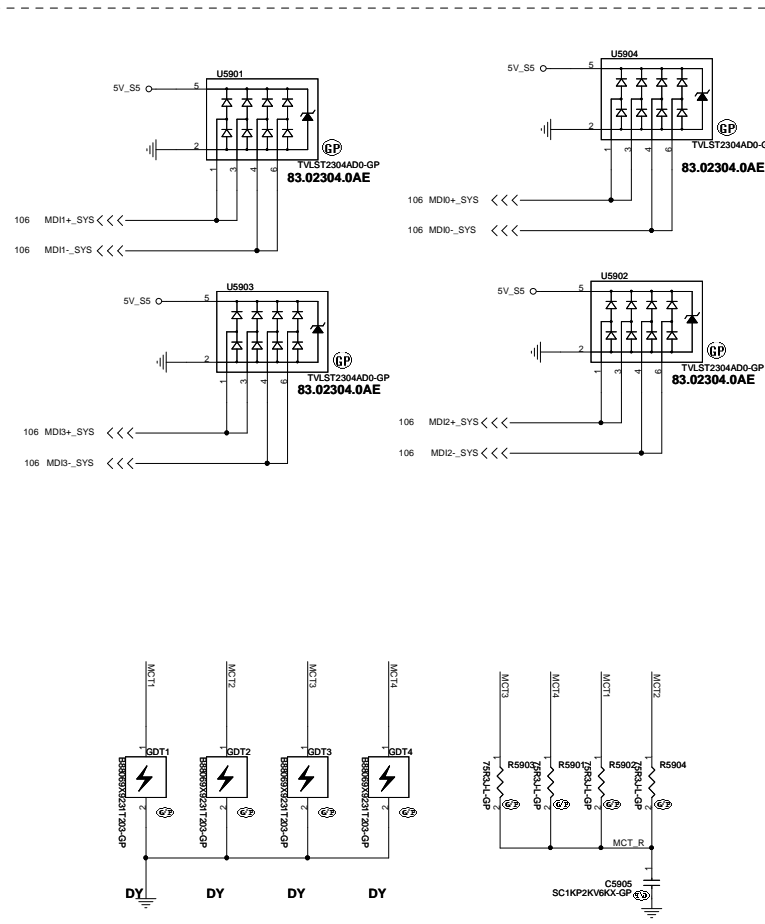
# GIGA Lan Transformer

SSID = LOM

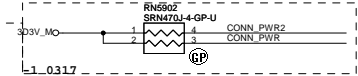
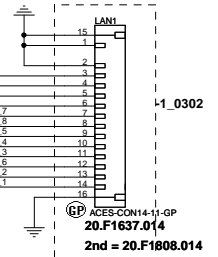
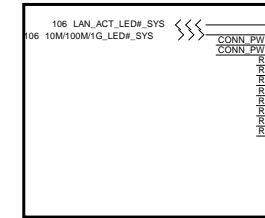
LAN MDI Off-Page



For EMI



LED COLOR  
10(+): 9(-)::GREEN  
12(+): 13(-)::ORANGE

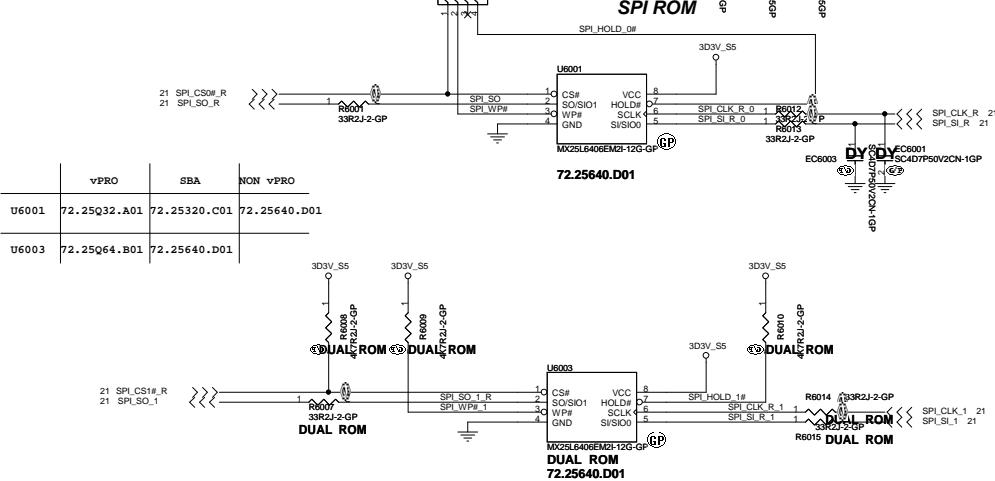


# SPI FLASH ROM (4M byte) for PCH

## SSID = Flash.ROM

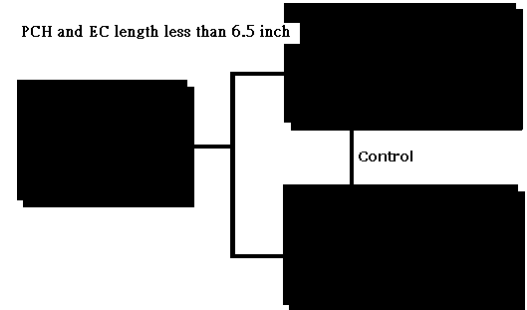
64MB: 72.25640.D01, 72.25Q64.B01  
32MB: 72.25Q32.A01, 72.25320.C01

### SYSTEM SPI ROM

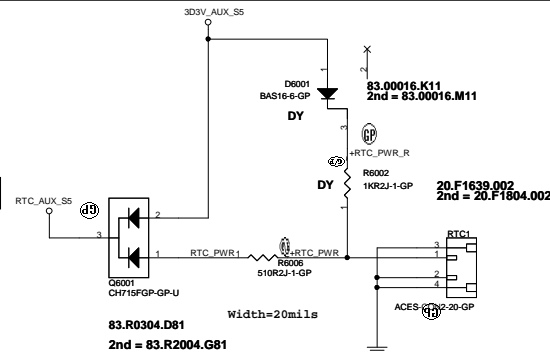


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



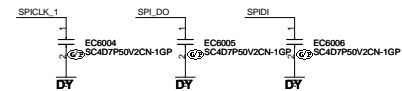
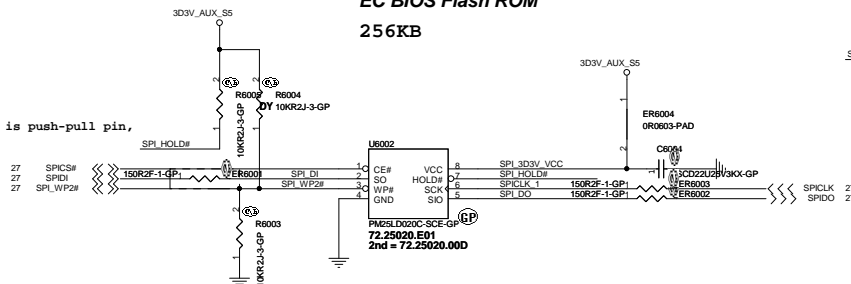
## SSID = RBATT



### EC BIOS Flash ROM

#### 256KB

for ENE FAE suggest, SPICs# is push-pull pin, don't need to pull high



Core Design

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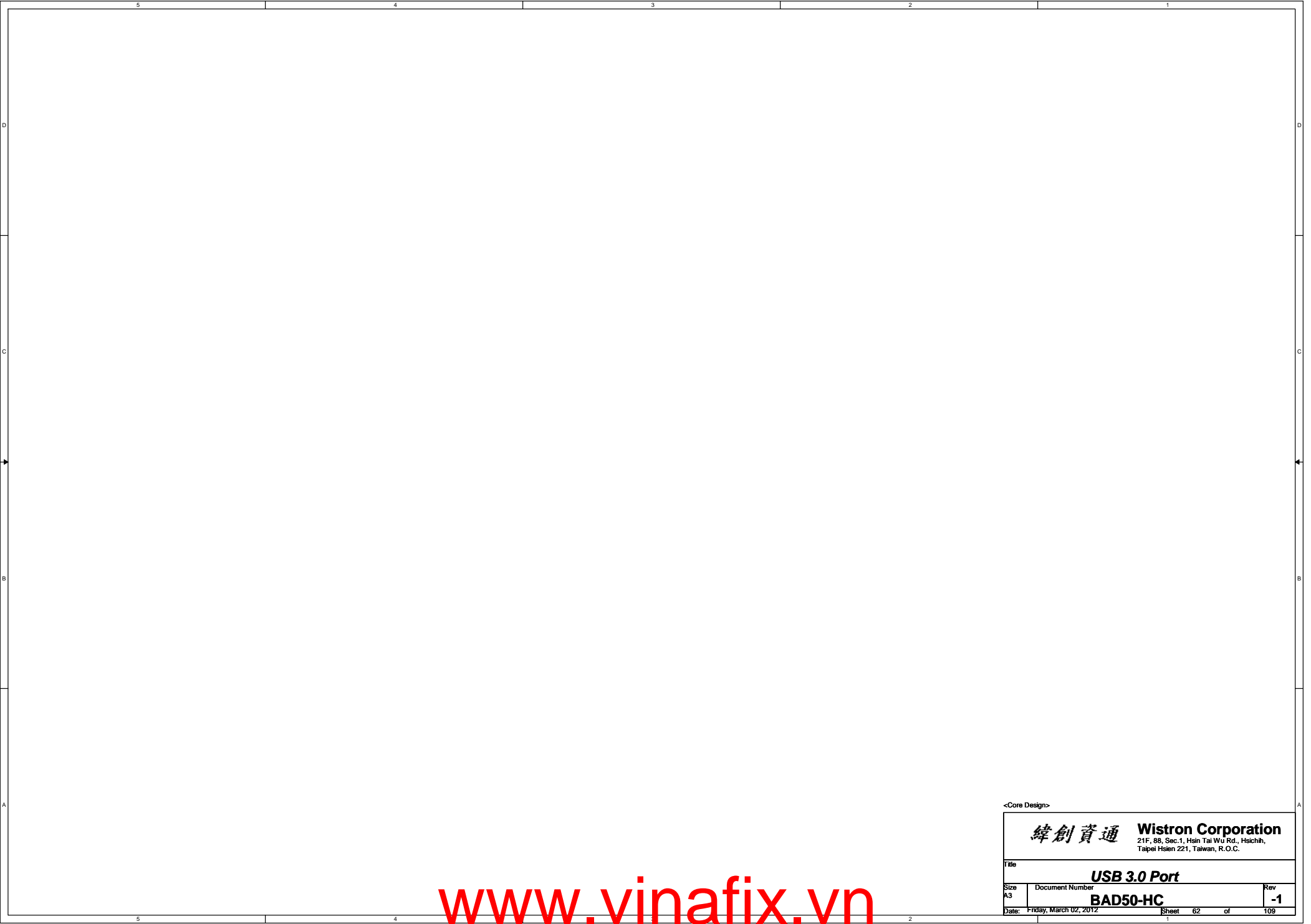
File	Flash/RTC		
Size	Document Number	BAD50-HC	Rev -1
Date	Thursday, March 29, 2012	Sheet 60	of 109



SSID = USB

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Title		
USB Power SW		
Size	Document Number	Rev
A4	BAD50-HC	-1
Date:	Friday, March 02, 2012	Sheet 61 of 109



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<Core Design>		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
USB 3.0 Port		
Size	Document Number	Rev
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SSID = User.Interface  
Bluetooth Module conn.

1220 SB del

EC6302 put near BLUE1 / all USB put one  
choke near connector by EMI request

## *ANNIE Bluetooth Module*

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Title

**Bluetooth**

Size  
A4

Document Number

**BAD50-HC**

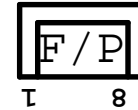
Rev  
-1

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Finger printer

JE40 delete FP function



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Title

**RESERVED**

Size  
A4

Document Number

**BAD50-HC**

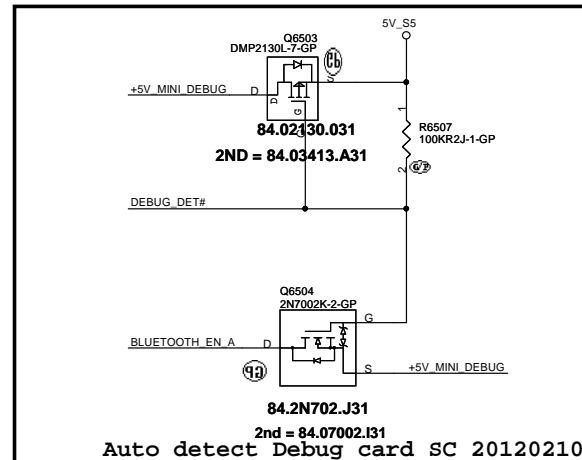
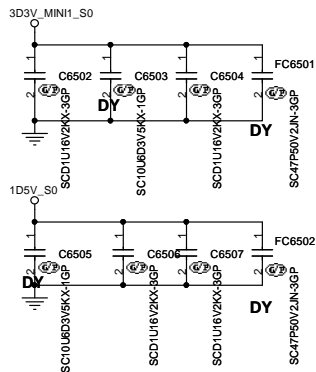
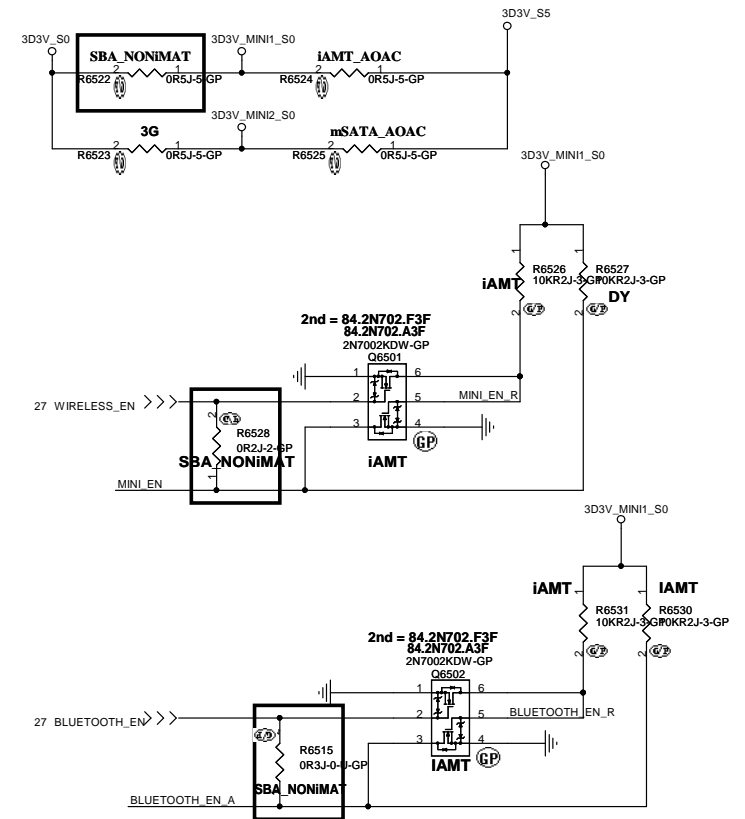
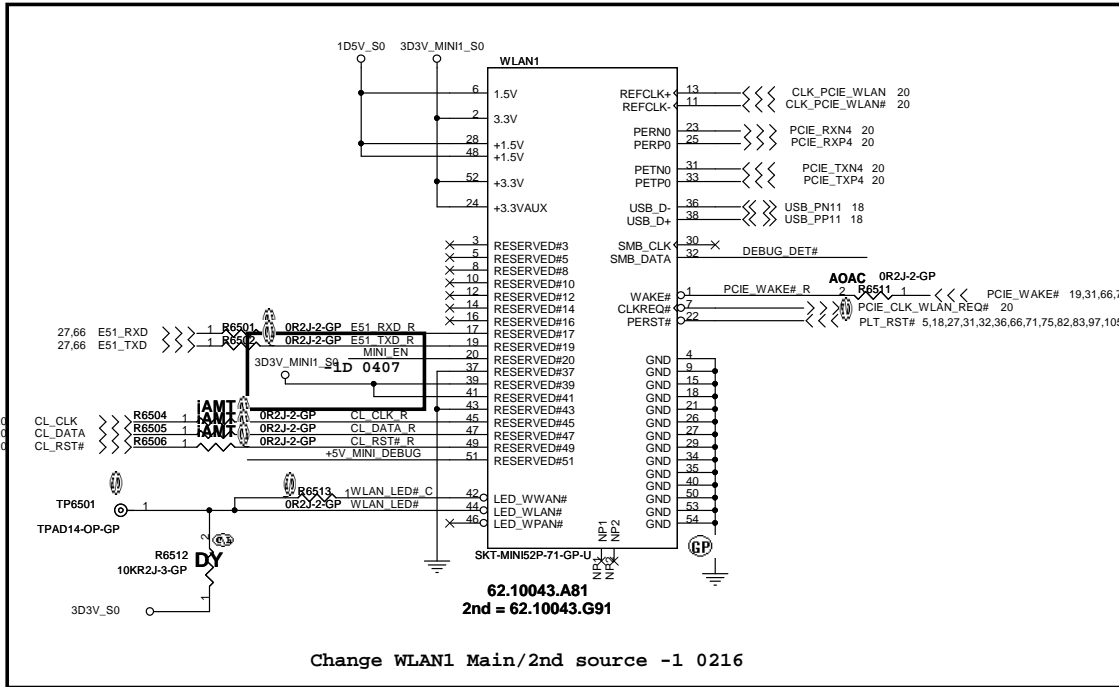
Rev  
**-1**

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SSID = Wireless

# Mini Card Connector(802.11a/b/g/n)





( Blanking )

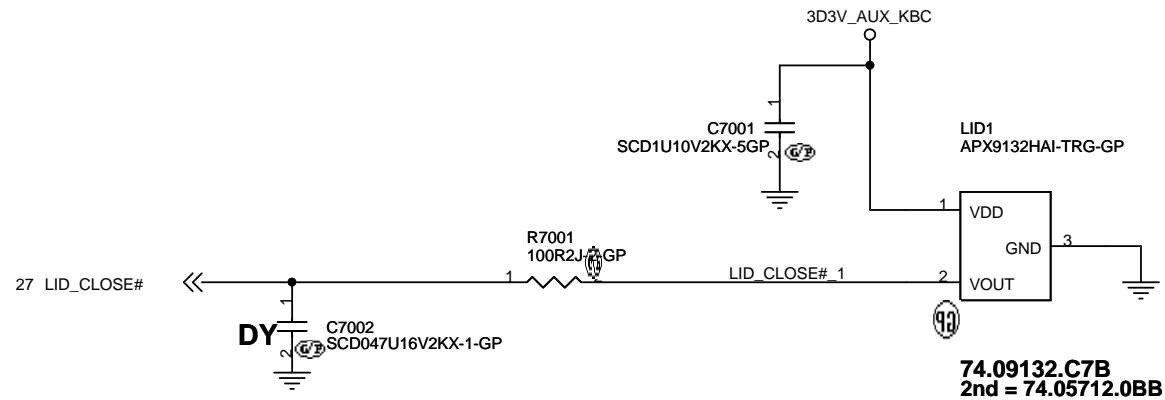
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Title			
Reserved			
Size	Document Number		Rev
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Title

**Hall Sensor**

Size  
A4

Document Number

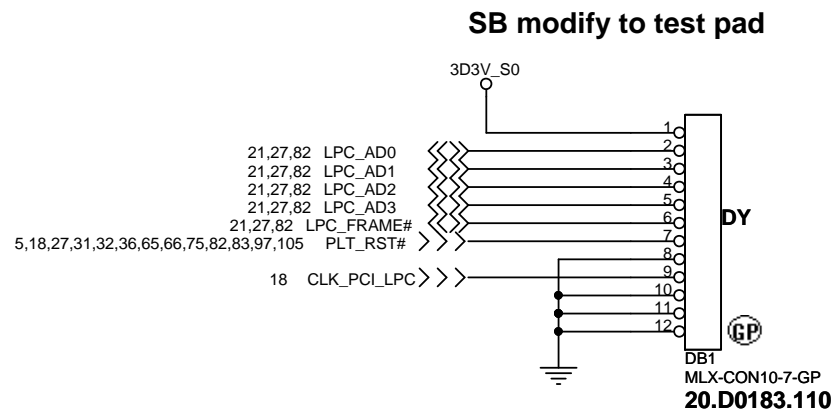
**BAD50-HC**

Rev  
-1

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Title

**Dubug connector**

Size  
A4

Document Number

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-1

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Title					
Reserved					
Size	Document Number				Rev
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Date:	Friday, March 02, 2012			Sheet	72 of 109

( Blanking )

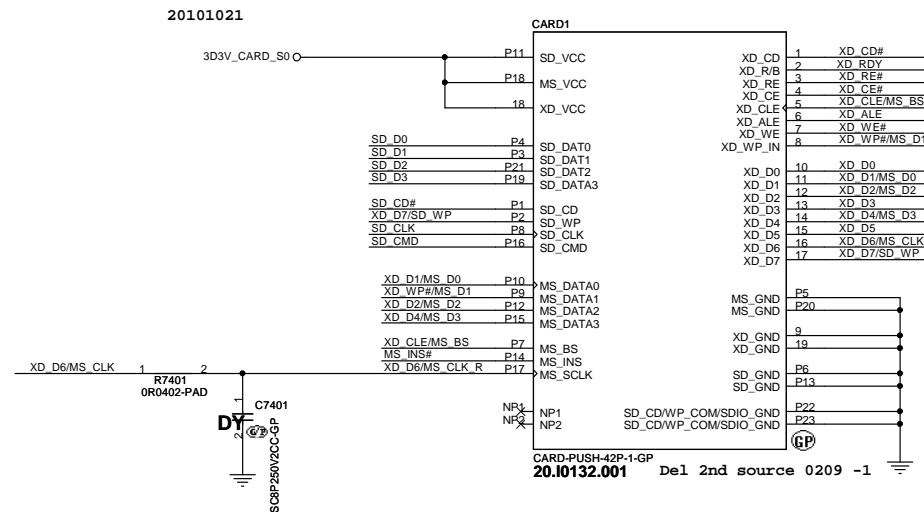
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Title			
Reserved			
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SSID = SDIO

# SD/XD/MS Card Reader

32 XD\_CD# << >> \_\_\_\_\_  
 32 SD\_D1 << >> \_\_\_\_\_  
 32 SD\_D0 << >> \_\_\_\_\_  
 32 SD\_D2 << >> \_\_\_\_\_  
 32 SD\_D3 << >> \_\_\_\_\_  
 32 SD\_CLK << >> \_\_\_\_\_  
 32 SD\_CMD << >> \_\_\_\_\_  
 32 SD\_CD# << >> \_\_\_\_\_  
 32 MS\_INS# << >> \_\_\_\_\_  
 32 XD\_RDY << >> \_\_\_\_\_ SP1(N0 SD\_D7)  
 32 XD\_RE# << >> \_\_\_\_\_ SP2(N0 SD\_D6)  
 32 XD\_CE# << >> \_\_\_\_\_ SP3(N0 SD\_D5)  
 32 XD\_WE# << >> \_\_\_\_\_ SP4(N0 SD\_D4)  
 32 XD\_CLE/MS\_BS << >> \_\_\_\_\_ SP5  
 32 XD\_ALE << >> \_\_\_\_\_ SP6  
 32 XD\_WP#/MS\_D1 << >> \_\_\_\_\_ SP7  
 32 XD\_D0 << >> \_\_\_\_\_ SP8(N0 MS\_D4)  
 32 XD\_D1/MS\_D0 << >> \_\_\_\_\_ SP9  
 32 XD\_D2/MS\_D2 << >> \_\_\_\_\_ SP10  
 32 XD\_D3 << >> \_\_\_\_\_ SP11(MS\_D6)  
 32 XD\_D4/MS\_D3 << >> \_\_\_\_\_ SP12  
 32 XD\_D5 << >> \_\_\_\_\_ SP13  
 32 XD\_D6/MS\_CLK << >> \_\_\_\_\_ SP14  
 32 XD\_D7/SD\_WP << >> \_\_\_\_\_ SP15



<Core Design>

緯創資通

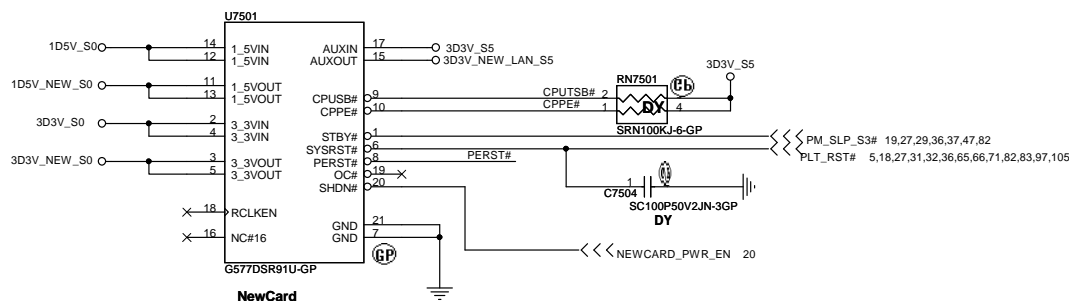
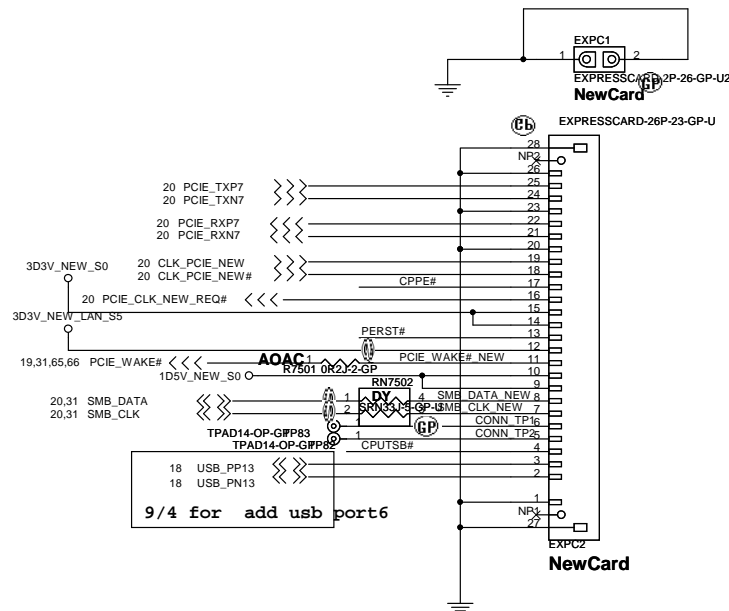
**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>CARD Reader CONN</b>	
Size	Document Number	Rev		
A3		<b>BAD50-HC</b>		-1
Date:	Saturday, March 03, 2012	Sheet	74	of 109

**SSID = ExpressCard**

For Expresscard socket

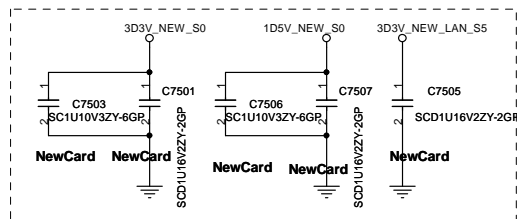
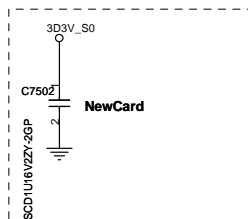
+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA



Place them Near to Chip

Place them Near to Connector

For EMI

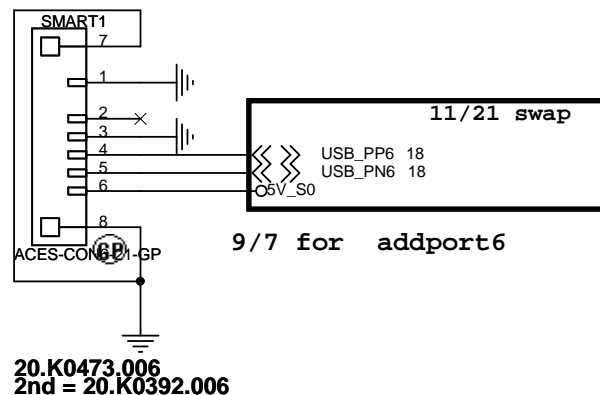


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Title			<b>New Card</b>	
Size	Document Number	Rev		
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Title

**Reserved**

Size  
A4

Document Number

**BAD50-HC**

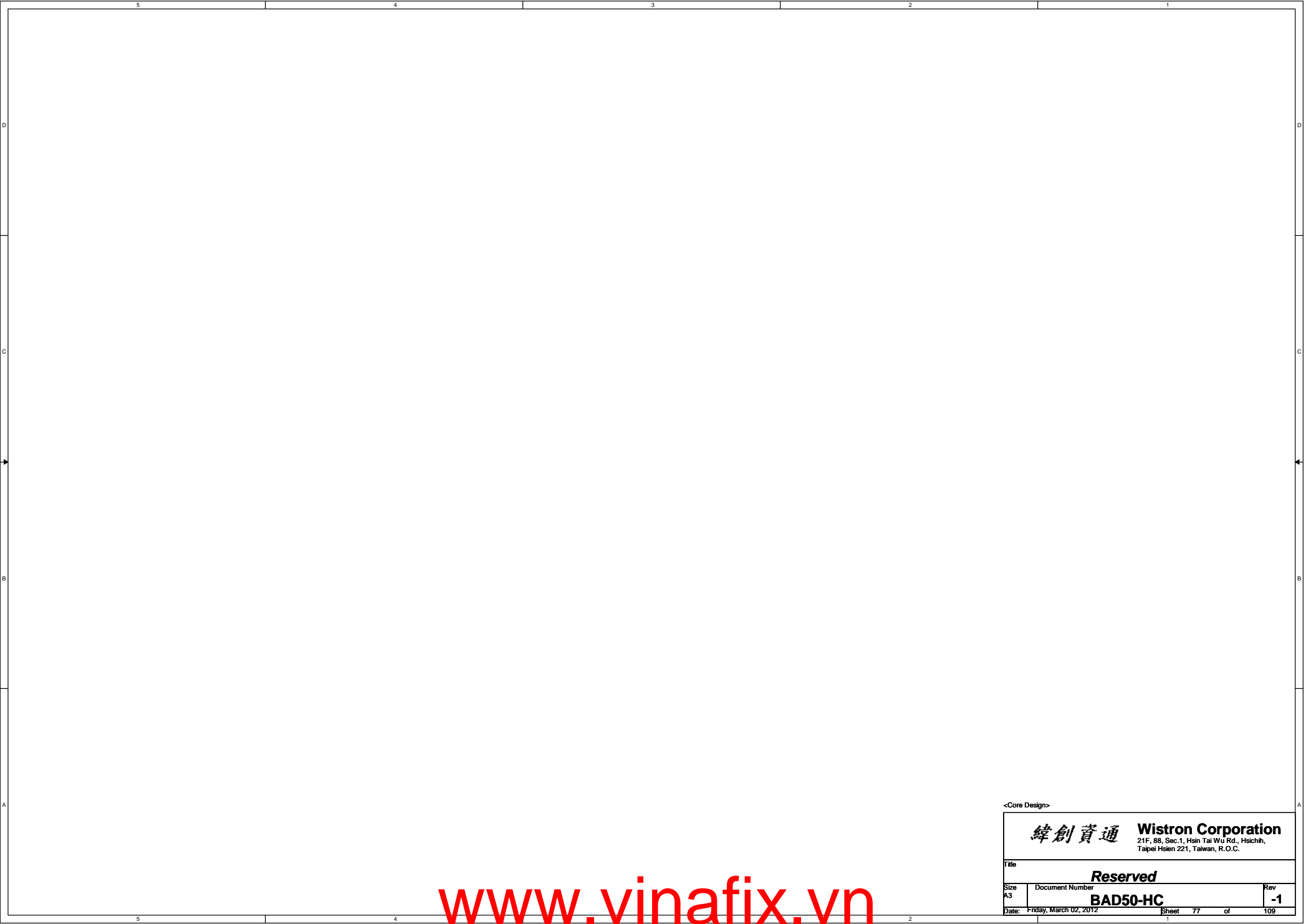
Rev

**-1**

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A3

Document Number  
BAD50-HC

Rev  
-1

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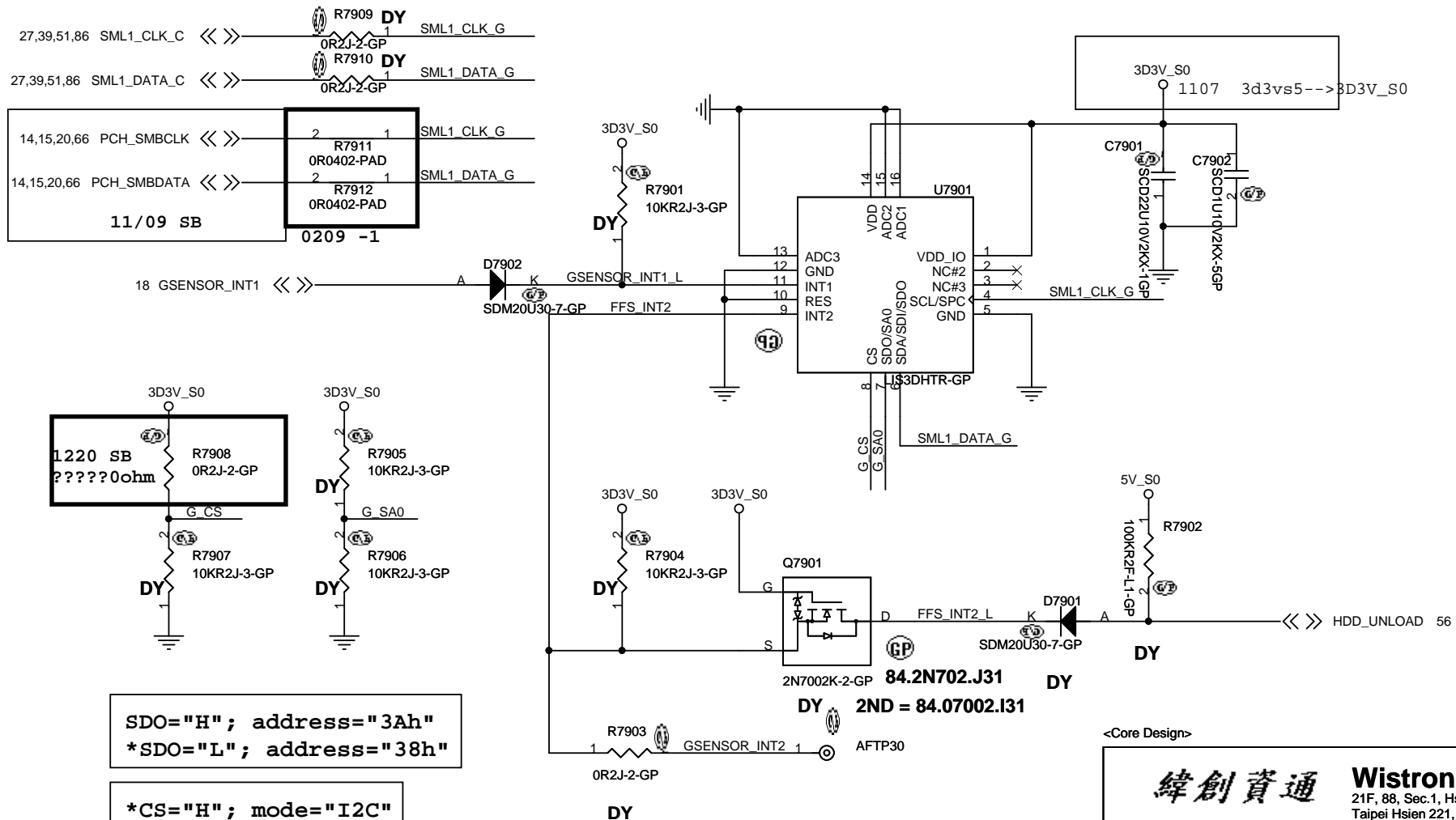
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
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SSID = User.Interface

## Free Fall Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



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Title

Free Fall Sensor

Size  
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Document Number

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( Blanking )

<Core Design>

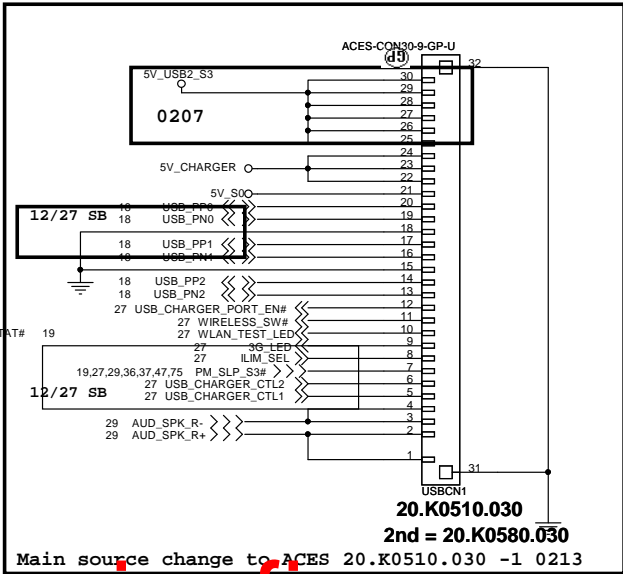
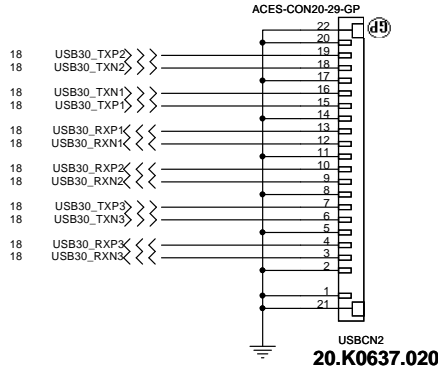
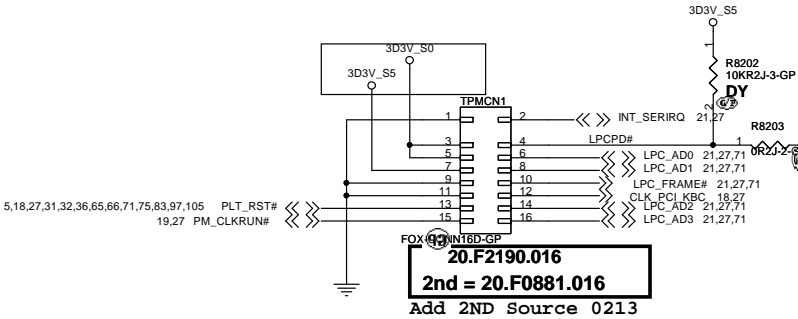
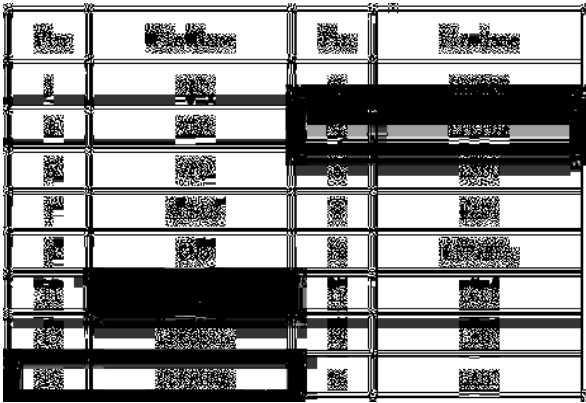
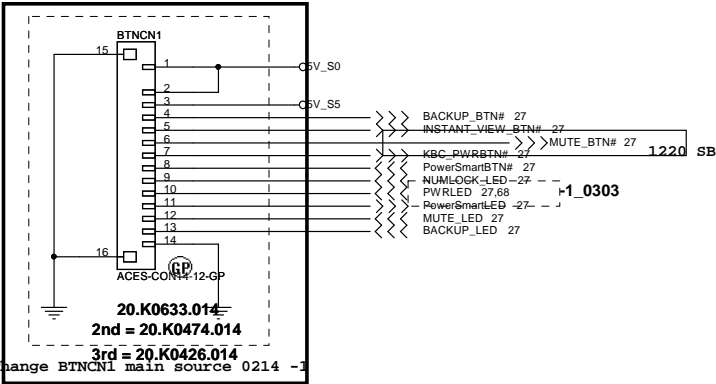
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	BAD50-HC	-1
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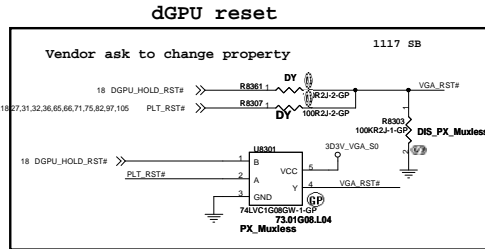
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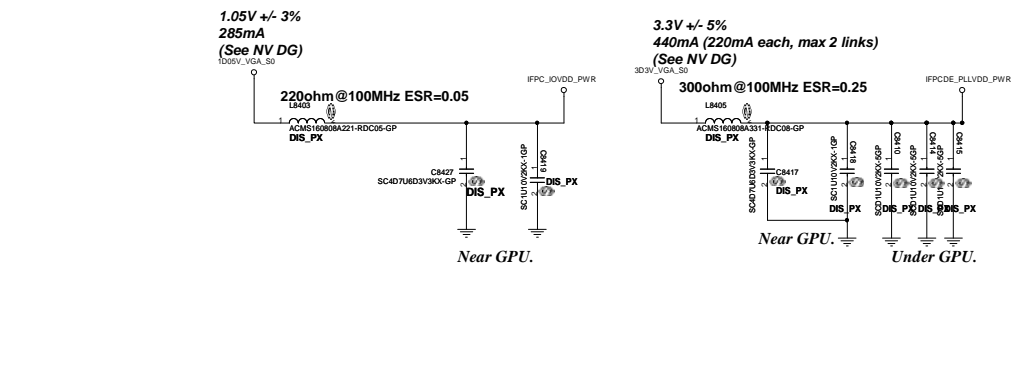
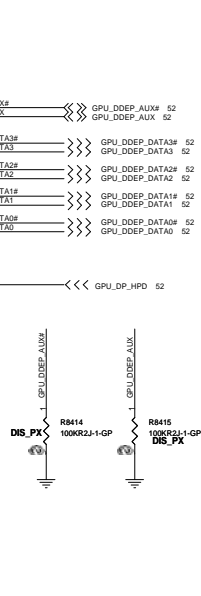
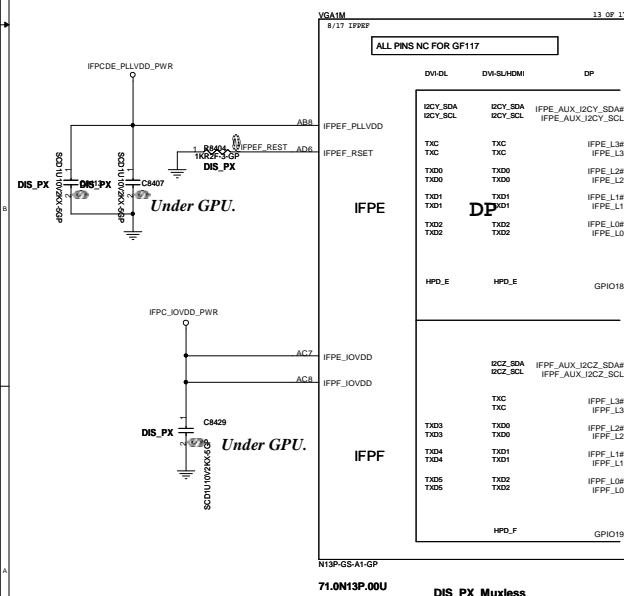
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Title		
Reserved		
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PWRCN1 FFC 異面

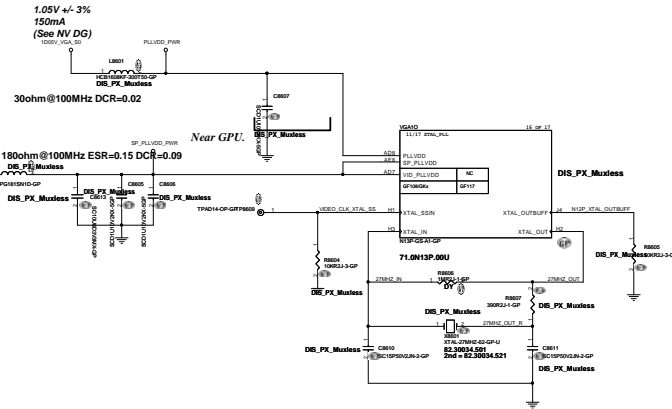












4.99 k	1000	0000
50.0 k	5001	0001
15.0 k	5010	0010
20.0 k	5011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
40.3 k	1111	0111

Table 109. Display Link to SDRx\_EXPOSED Bit Mapping

Node Link Mode	IPv4/6	SRID EXPOSED = 0	SRID EXPOSED = 0
Split Mode	EPIC	SRID EXPOSED = 1	SRID EXPOSED = 0
	EPD	SRID EXPOSED = 1	SRID EXPOSED = 0
	EPF	SRID EXPOSED = 1	SRID EXPOSED = 0
	EPH	SRID EXPOSED = 1	SRID EXPOSED = 0
Split Mode	IPv4/6		
	EPIC	SRID EXPOSED = 1	SRID EXPOSED = 0
	EPD	SRID EXPOSED = 1	SRID EXPOSED = 0
	EPF	SRID EXPOSED = 1	SRID EXPOSED = 0

Table 106. 3GIO\_PADCFG Strap Setting

0000-0101	RESERVED	
0110	Heat exchanger	Heat exchanger: Oil/water
0011-1111	RESERVED	

	ROM_SI	ROM_SO	ROM_CLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P_GS ES	PH 10K ohm	PH 4.99K ohm	PH 45K.3ohm	PL 34.8K ohm	PH 20K ohm	PH 15K ohm	PL 20K ohm	PH 20K ohm
N13P_GL	PH 10K ohm	PL 15K ohm	PH 45K.3ohm	PL 34.8K ohm	PH 10K ohm	PH 15K ohm	PH 20K ohm	PH 20K ohm

STRAP0	USER[0]=1		STRAP1	3GIO_PADCFG[0]=0	
	USER[1]=1			3GIO_PADCFG[1]=1	
	USER[2]=1			3GIO_PADCFG[2]=1	
	USER[3]=1			3GIO_PADCFG[3]=0	
		<b>USE 1111 (45K)</b>			<b>USE 0110 (35K)</b>

Table 105. User Straps

0000	BCA	1024 x 768	-/-	
0001	BCA	1024 x 768	+/+	
0010	WGA	1280 x 1024	-/-	
0011	WGA+	1400 x 1024	-/-	
0100	WGA	1600 x 1200	+/+	
0101	WGA	1600 x 1200	-/-	
0110	WGA+	1600 x 1200	-/-	
0111	WGA	800 x 600	-/-	
0000 + 0100				Continuous refresh
1111				Continuous refresh (Default)

ROM_2G	Hynix 2G 0110 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 2G 0011 128*16*8 800MHZ
ROM_SI R8627	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

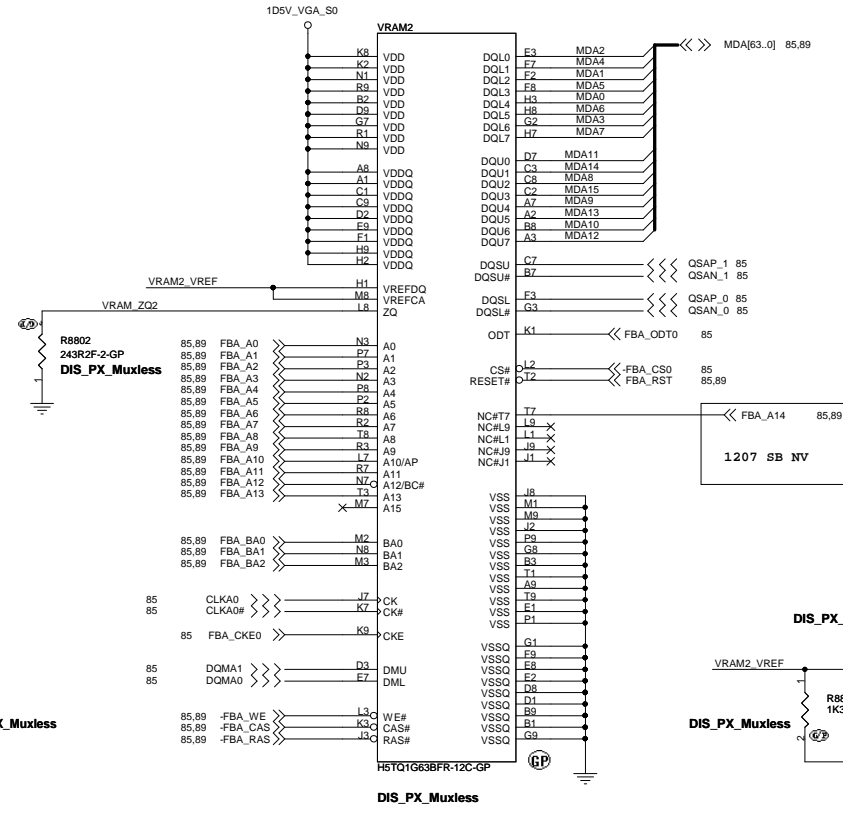
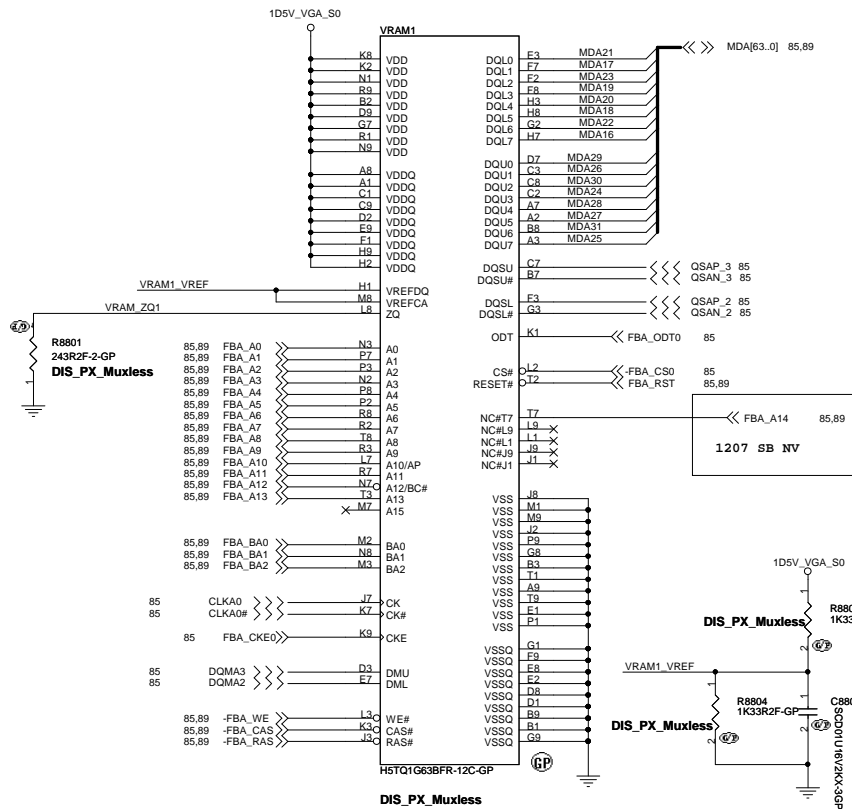
	N13P-GS DEV ID: 0x0FD2	N13P-GS-ES DEV ID: 0x0FDB	N13P-GL DEV ID: 0x0DE9		
STRAP2	15Kohm 64.15026.6DL	20Kohm 64.20025.6DL	10Kohm 63.10334.1DL		

	DEVID	ROM CLK	END
[REDACTED]			
MLSP-02-A1	000002	1000-014500	0010-001500

[illegible]

Study/No. Sites	Logical strapping number 0-1001	Logical strapping number 0-1001	Logical strapping number 0-1001	Logical strapping number 0-1001	
1	0	0	0	0	02.1.000
2	1	1	1	1	02.1.001
3	0	0	0	0	02.1.002
4	1	0	0	1	02.1.003
5	1	1	1	1	02.1.004
6	0	1	1	0	02.1.005
7	1	0	1	0	02.1.006
8	1	0	1	0	02.1.007
9	0	1	1	0	02.1.008
10	1	0	1	0	02.1.009
11	0	1	1	0	02.1.010
12	1	0	1	0	02.1.011
13	0	1	1	0	02.1.012
14	1	0	1	0	02.1.013
15	0	1	1	0	02.1.014
16	1	0	1	0	02.1.015
17	0	1	1	0	02.1.016
18	1	0	1	0	02.1.017
19	0	1	1	0	02.1.018
20	1	0	1	0	02.1.019
21	0	1	1	0	02.1.020
22	1	0	1	0	02.1.021
23	0	1	1	0	02.1.022
24	1	0	1	0	02.1.023
25	0	1	1	0	02.1.024
26	1	0	1	0	02.1.025
27	0	1	1	0	02.1.026
28	1	0	1	0	02.1.027
29	0	1	1	0	02.1.028
30	1	0	1	0	02.1.029
31	0	1	1	0	02.1.030
32	1	0	1	0	02.1.031
33	0	1	1	0	02.1.032
34	1	0	1	0	02.1.033
35	0	1	1	0	02.1.034
36	1	0	1	0	02.1.035
37	0	1	1	0	02.1.036
38	1	0	1	0	02.1.037
39	0	1	1	0	02.1.038
40	1	0	1	0	02.1.039
41	0	1	1	0	02.1.040
42	1	0	1	0	02.1.041
43	0	1	1	0	02.1.042
44	1	0	1	0	02.1.043
45	0	1	1	0	02.1.044
46	1	0	1	0	02.1.045
47	0	1	1	0	02.1.046
48	1	0	1	0	02.1.047
49	0	1	1	0	02.1.048
50	1	0	1	0	02.1.049
51	0	1	1	0	02.1.050
52	1	0	1	0	02.1.051
53	0	1	1	0	02.1.052
54	1	0	1	0	02.1.053
55	0	1	1	0	02.1.054
56	1	0	1	0	02.1.055
57	0	1	1	0	02.1.056
58	1	0	1	0	02.1.057
59	0	1	1	0	02.1.058
60	1	0	1	0	02.1.059
61	0	1	1	0	02.1.060
62	1	0	1	0	02.1.061
63	0	1	1	0	02.1.062
64	1	0	1	0	02.1.063
65	0	1	1	0	02.1.064
66	1	0	1	0	02.1.065
67	0	1	1	0	02.1.066
68	1	0	1	0	02.1.067
69	0	1	1	0	02.1.068
70	1	0	1	0	02.1.069

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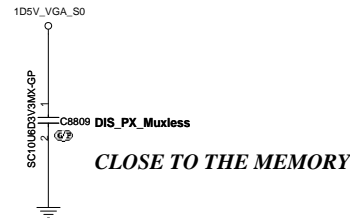
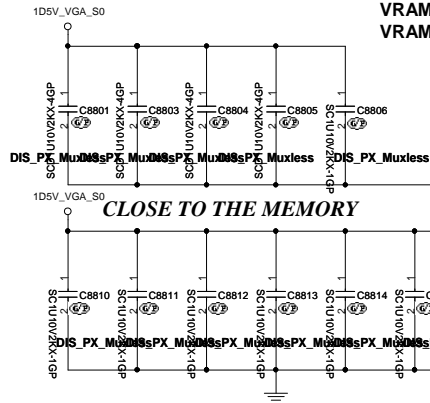


Hy2GX8\_VR.2GB0G.001,Sam1GX8\_VR.1GB0B.006,,Hy1GX8\_72.51G63.C0U,Sam512X4\_VR.1GB0B.006,Sam2GX8

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2GX8  
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006  
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



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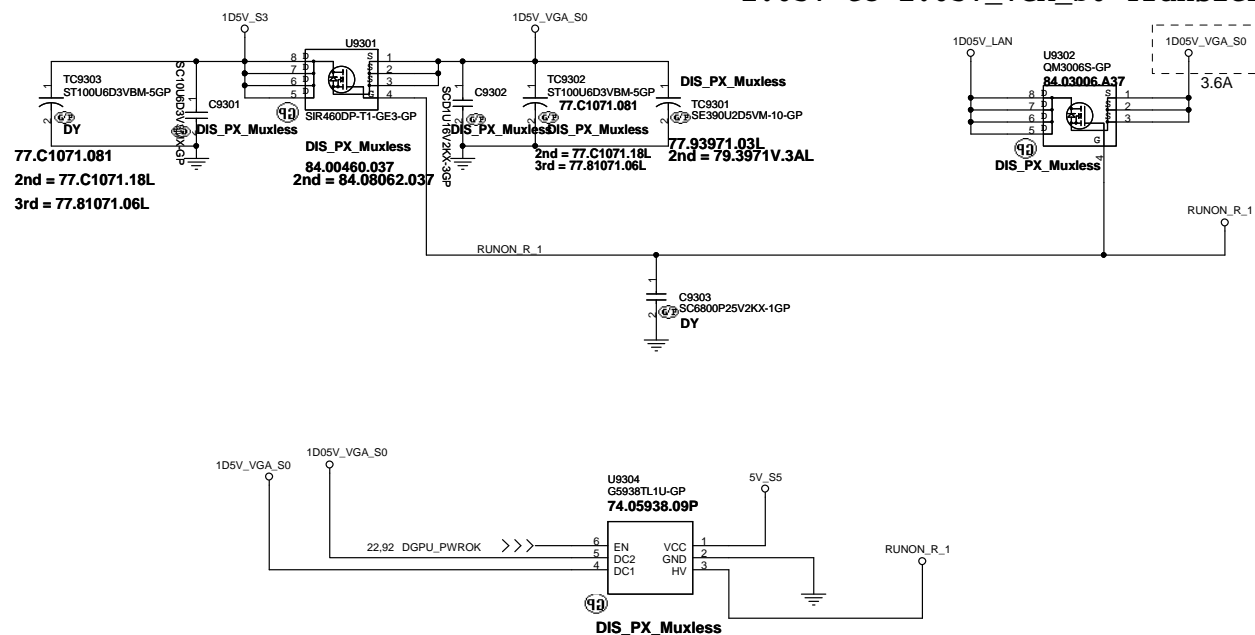






## 1D5V\_VGA\_S0

## 1.05V to 1.05V\_VGA\_S0 Transfer



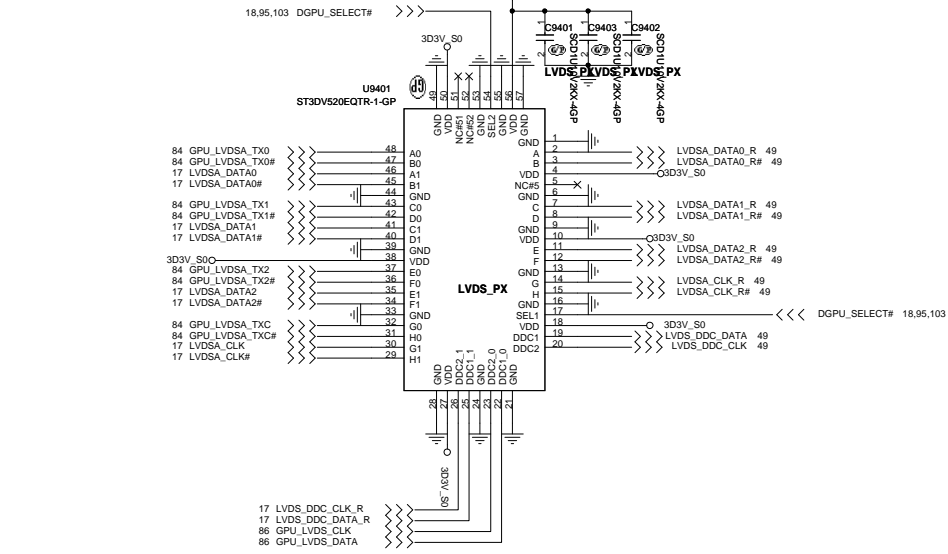
1D8V\_S0\_NV = IFPA\_IOVDD & IFPB\_IOVDD, it should be the latest ramp up rail.

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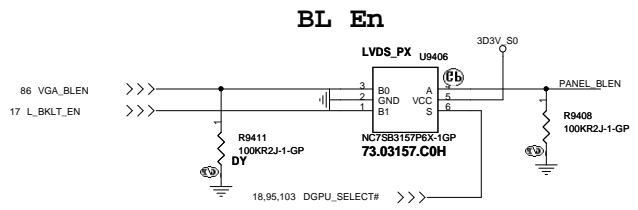
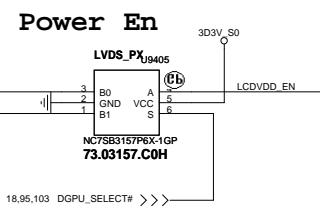
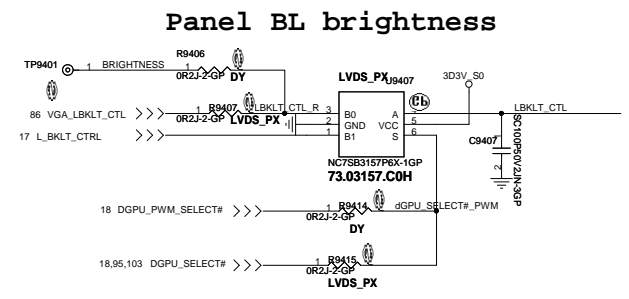
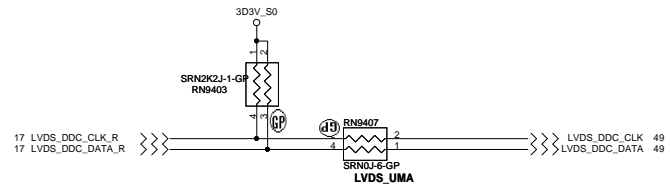
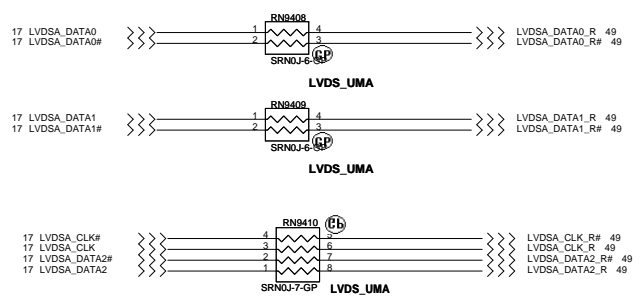
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<b>DISCRETE VGA POWER</b>			
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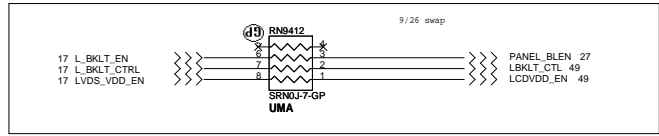
LVDS



SEL->L(X=nX0),H(X=nX1)  
SEL1 Control A~H  
SEL2 Control DDC1,DDC2



Panel BL brightness/Power En/BL En

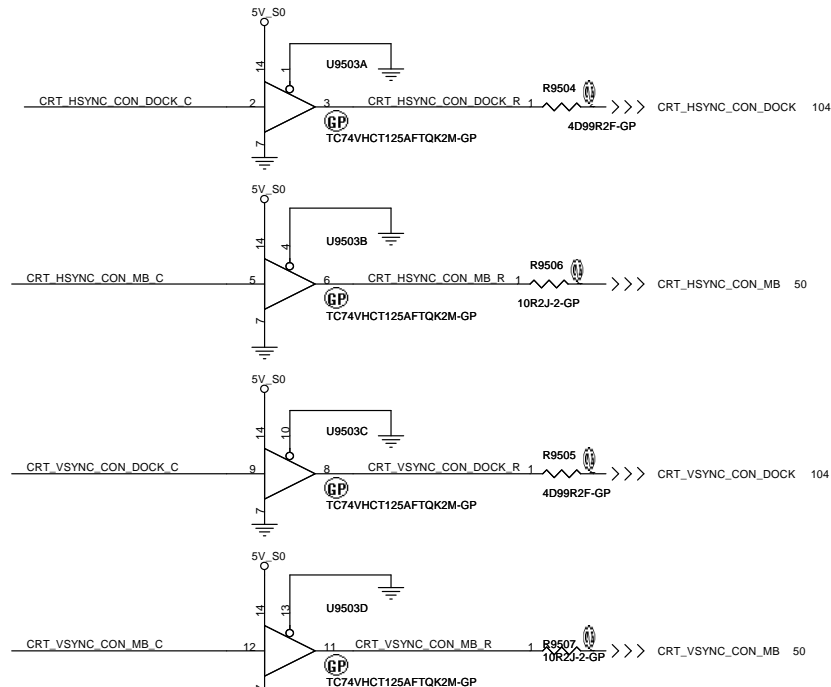
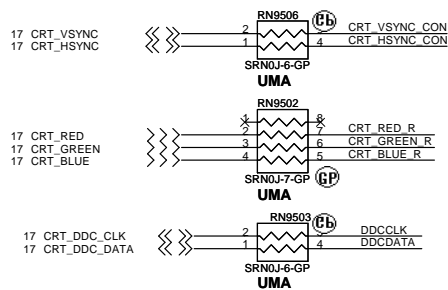
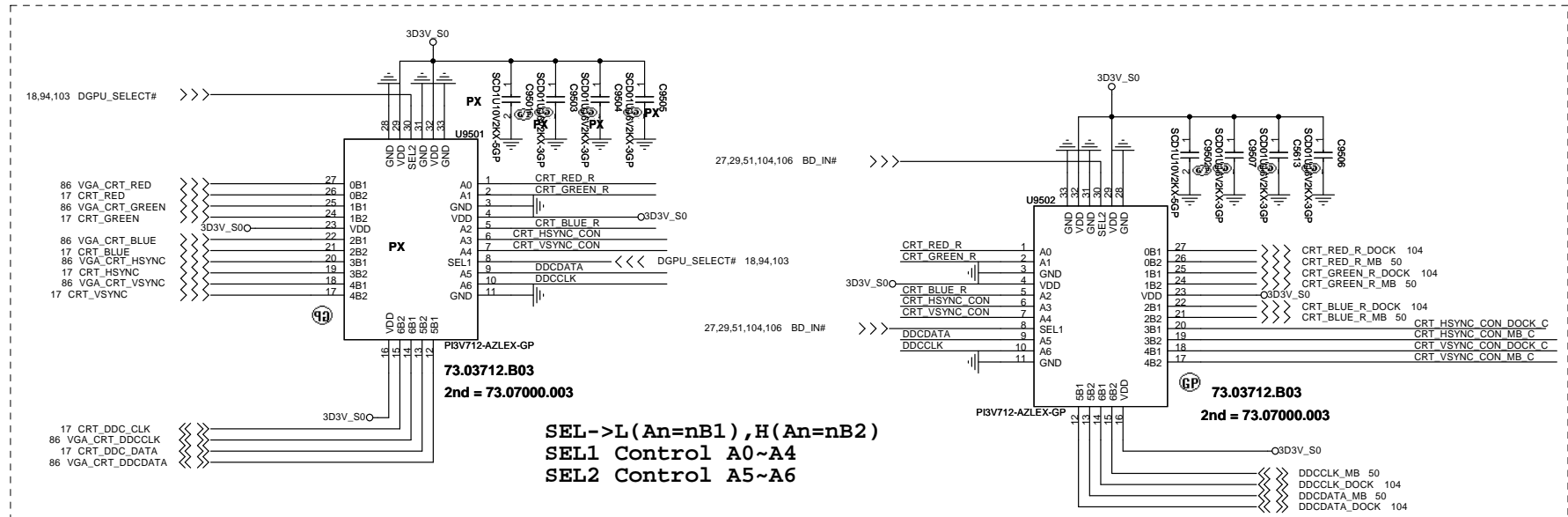


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## CRT DDCDATA & DDCCLK

VDD :

Recommend to use 6 caps ( $0.1\mu + 5 \times 10\text{nF}$ ) close to our chips



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1	Title
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### CRT\_Switch

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A3

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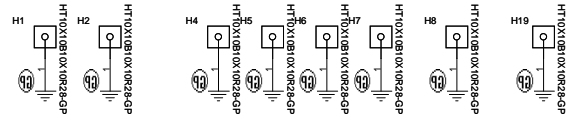
Rev	-1
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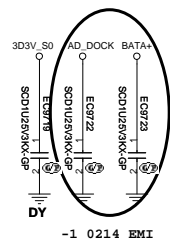
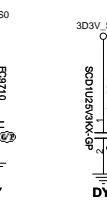
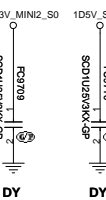
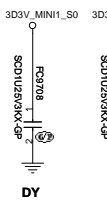
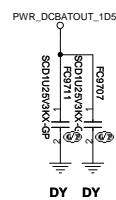
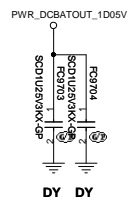
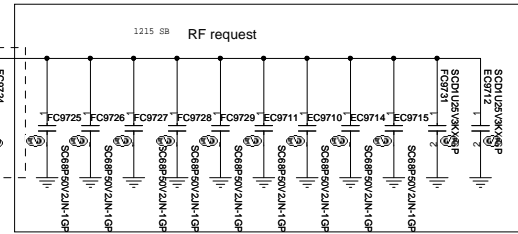
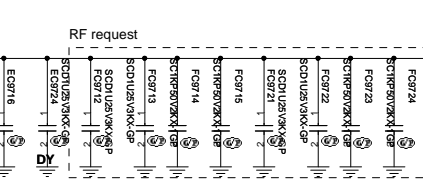
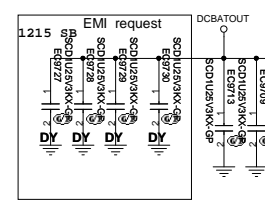
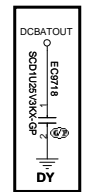
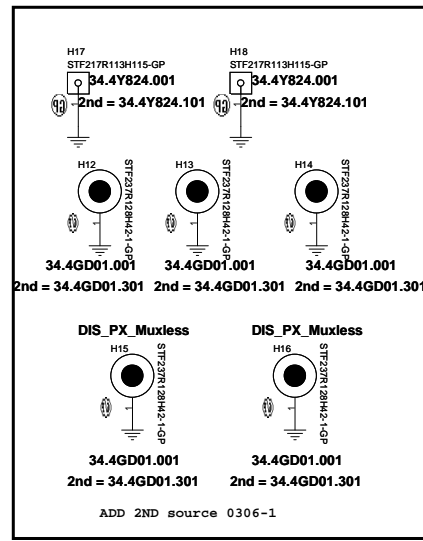
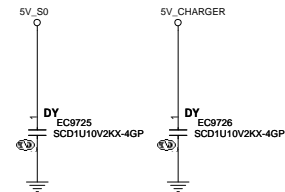
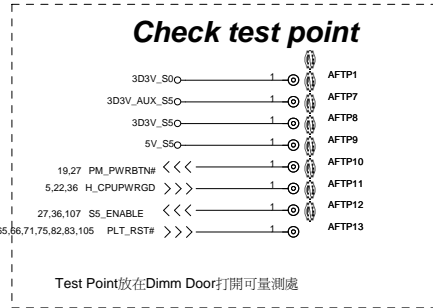
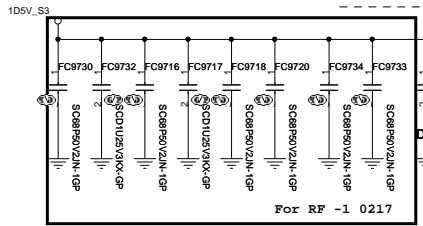
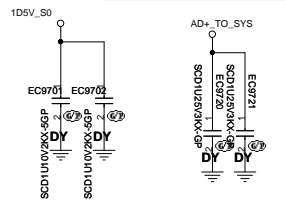
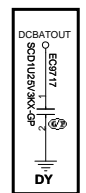
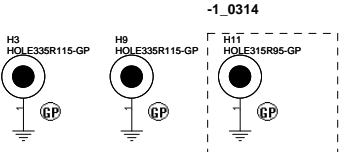
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SSID = SDIO

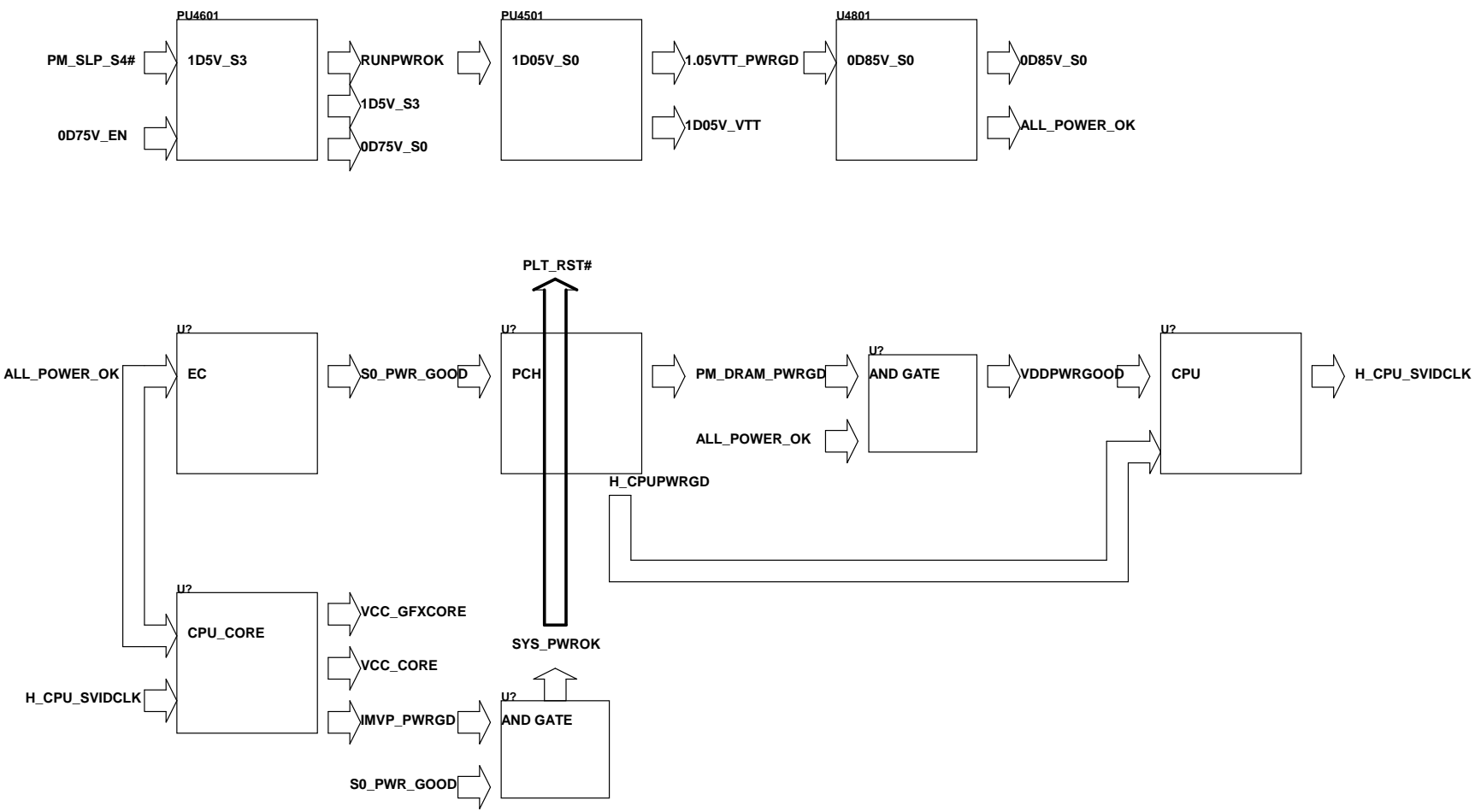
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DEL Spring -1 0213

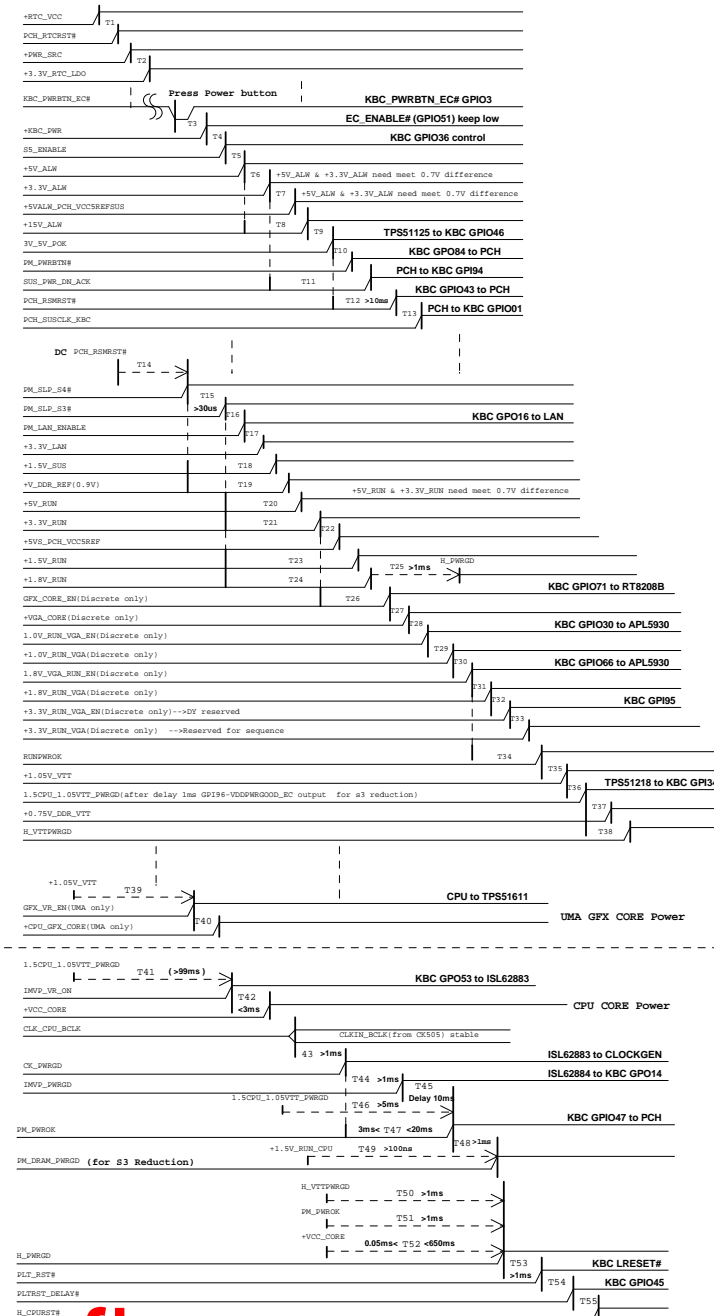


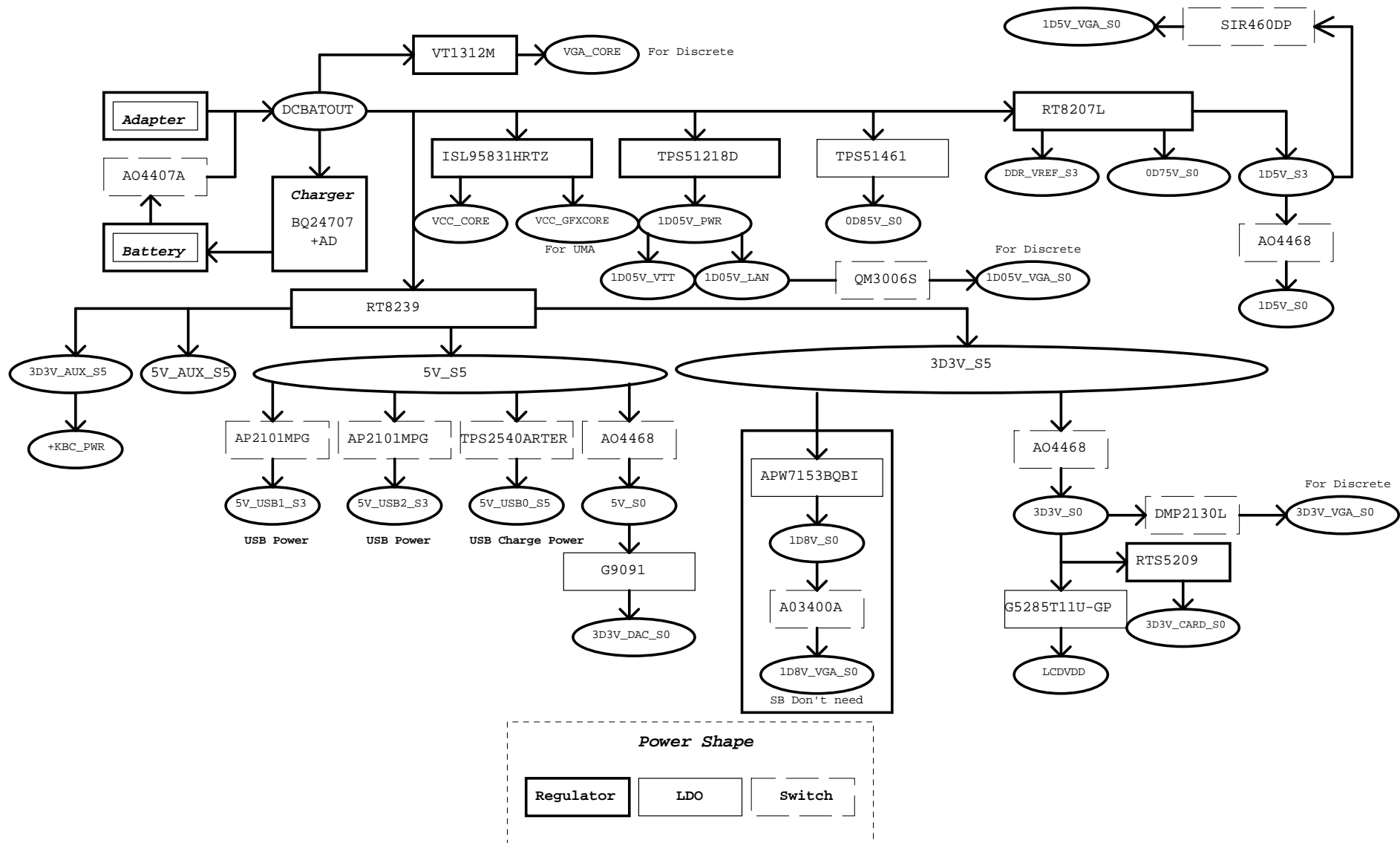
Power Sequence



**(AC mode)**

red word: KBC GPIO





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**Power Block Diagram**

Size

Document Number

**BAD50-HC**

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**-1**

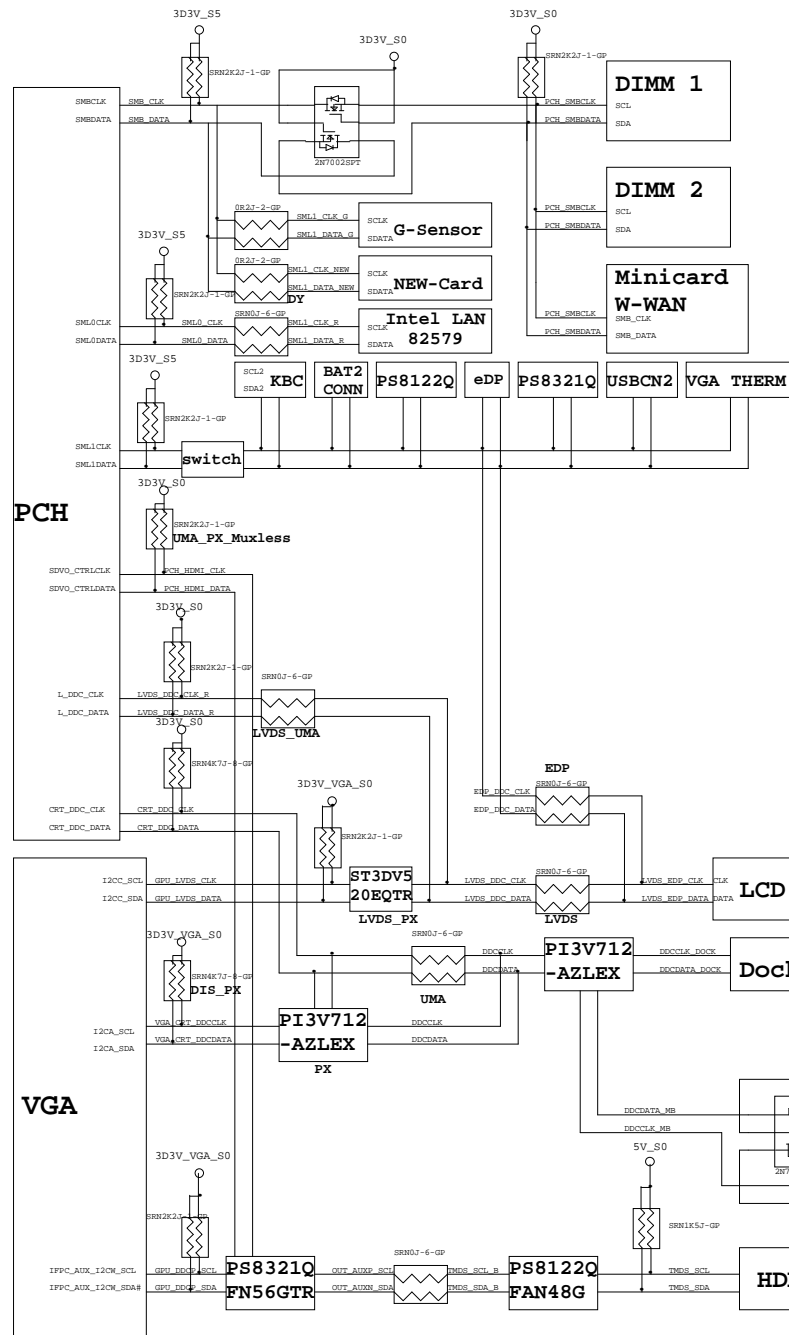
Date: Saturday, March 03, 2012

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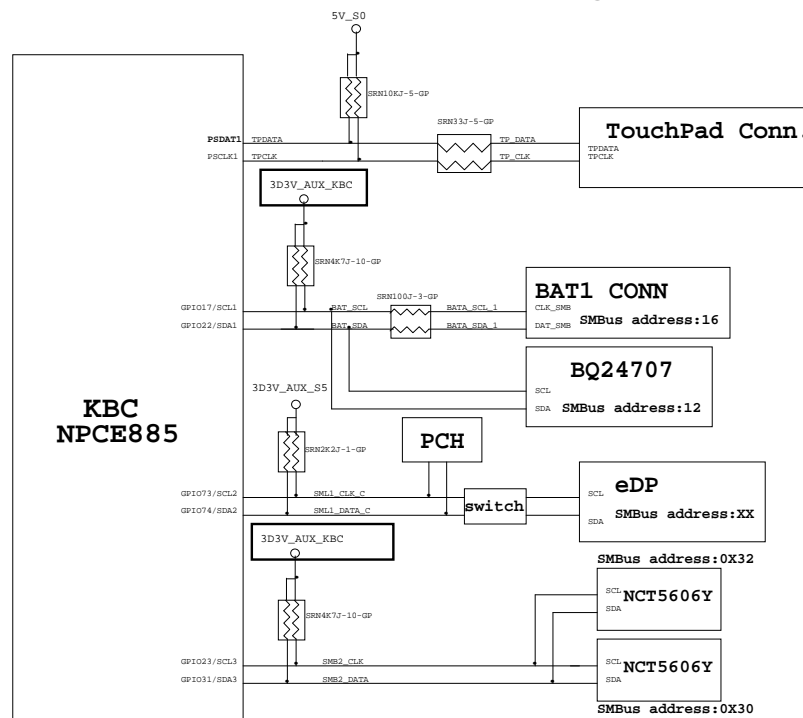
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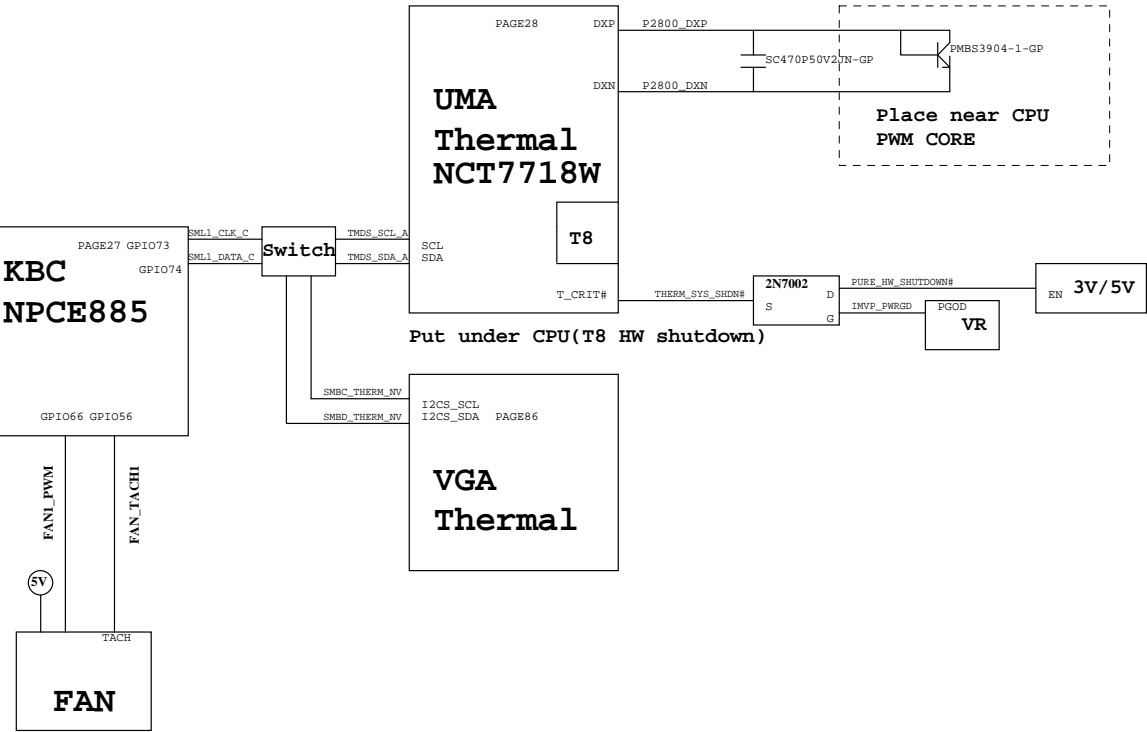
# PCH SMBus Block Diagram



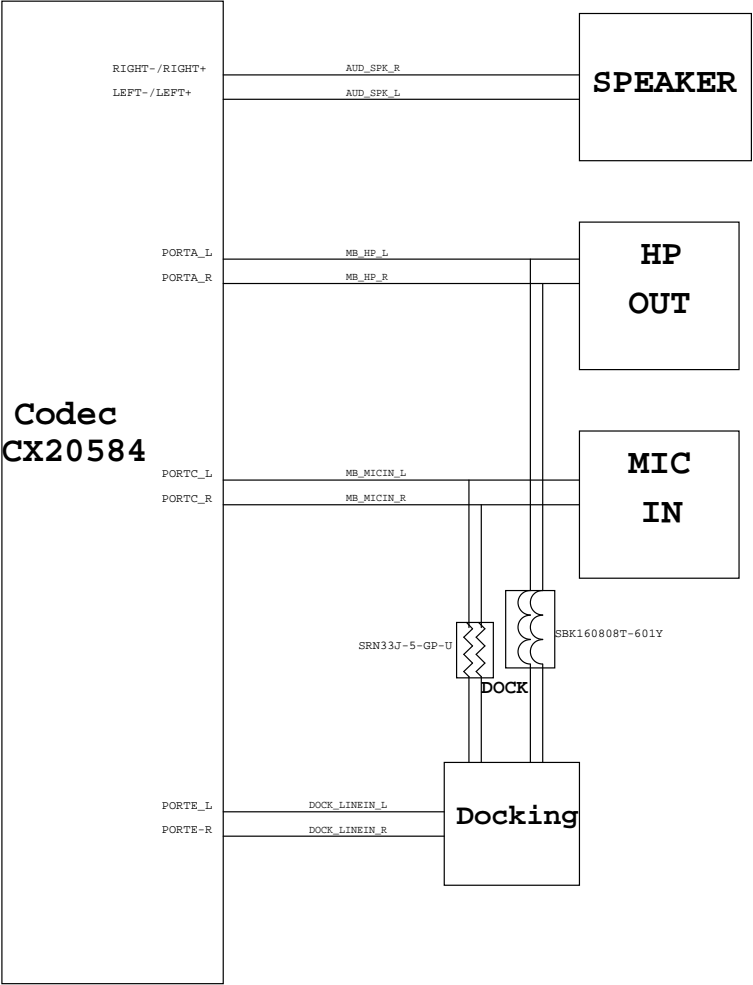
# KBC SMBus Block Diagram

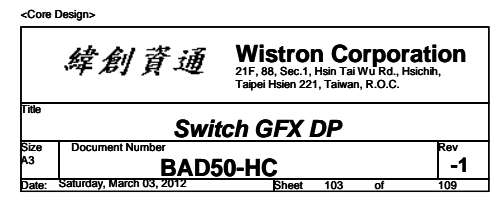
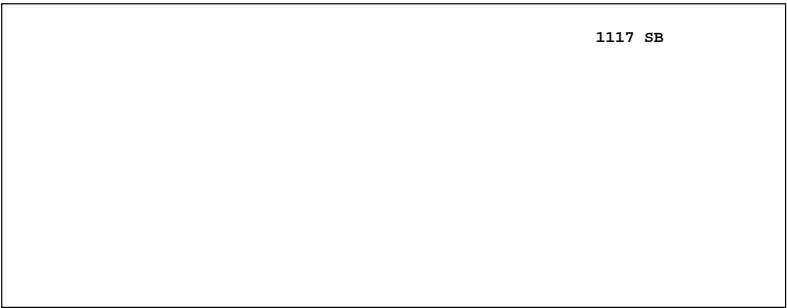


# Thermal Block Diagram



# Audio Block Diagram

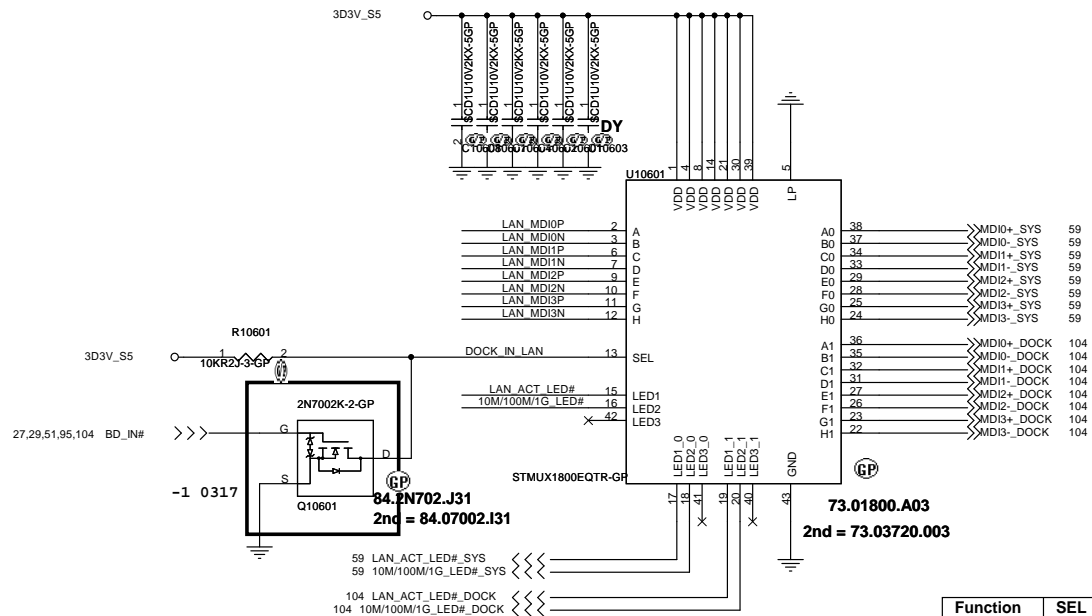
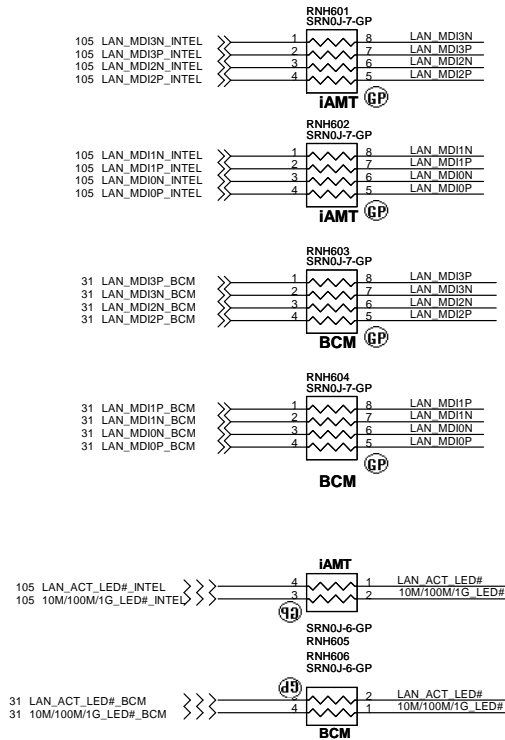








## LAN switch

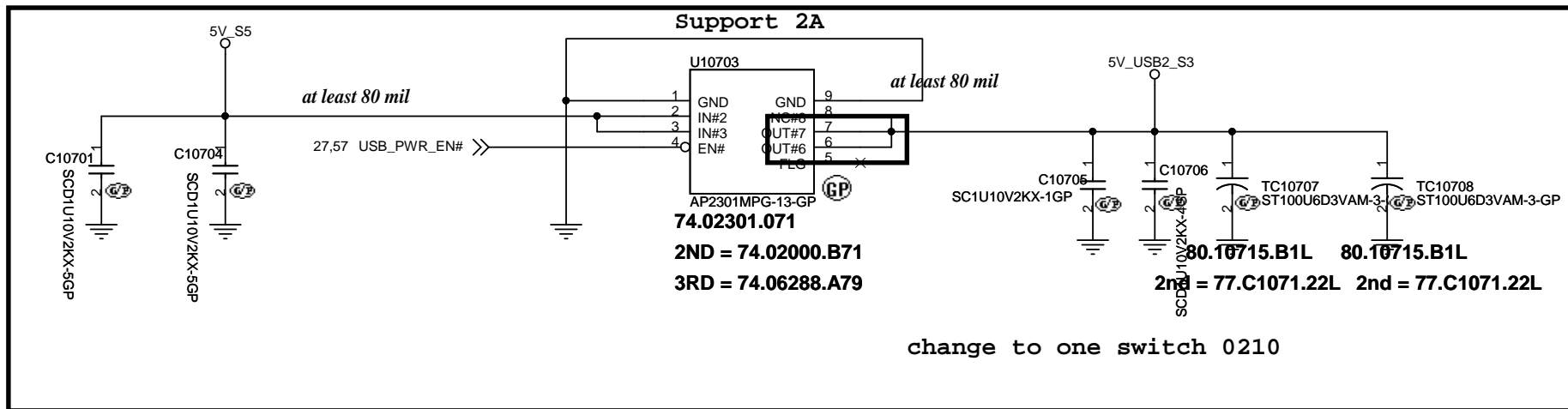
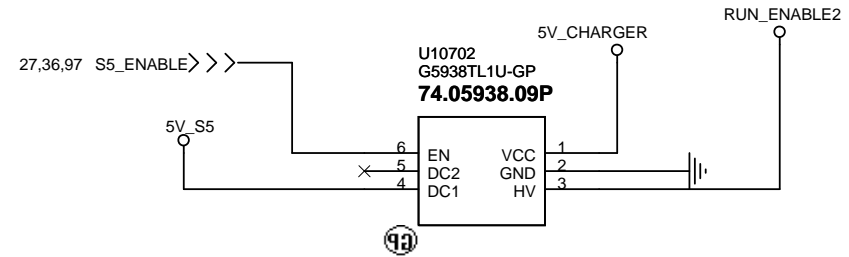
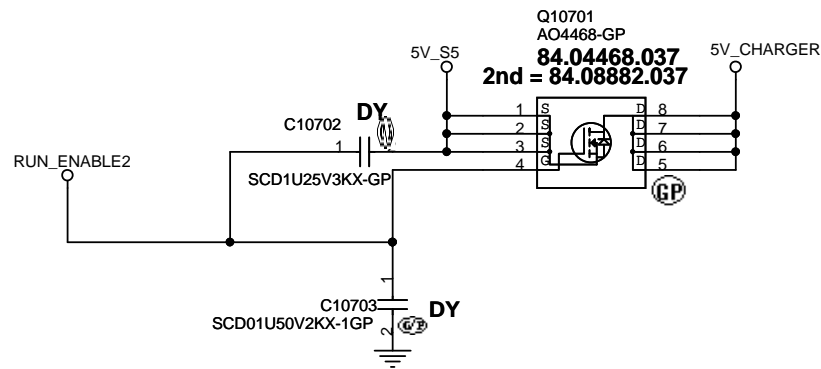


Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

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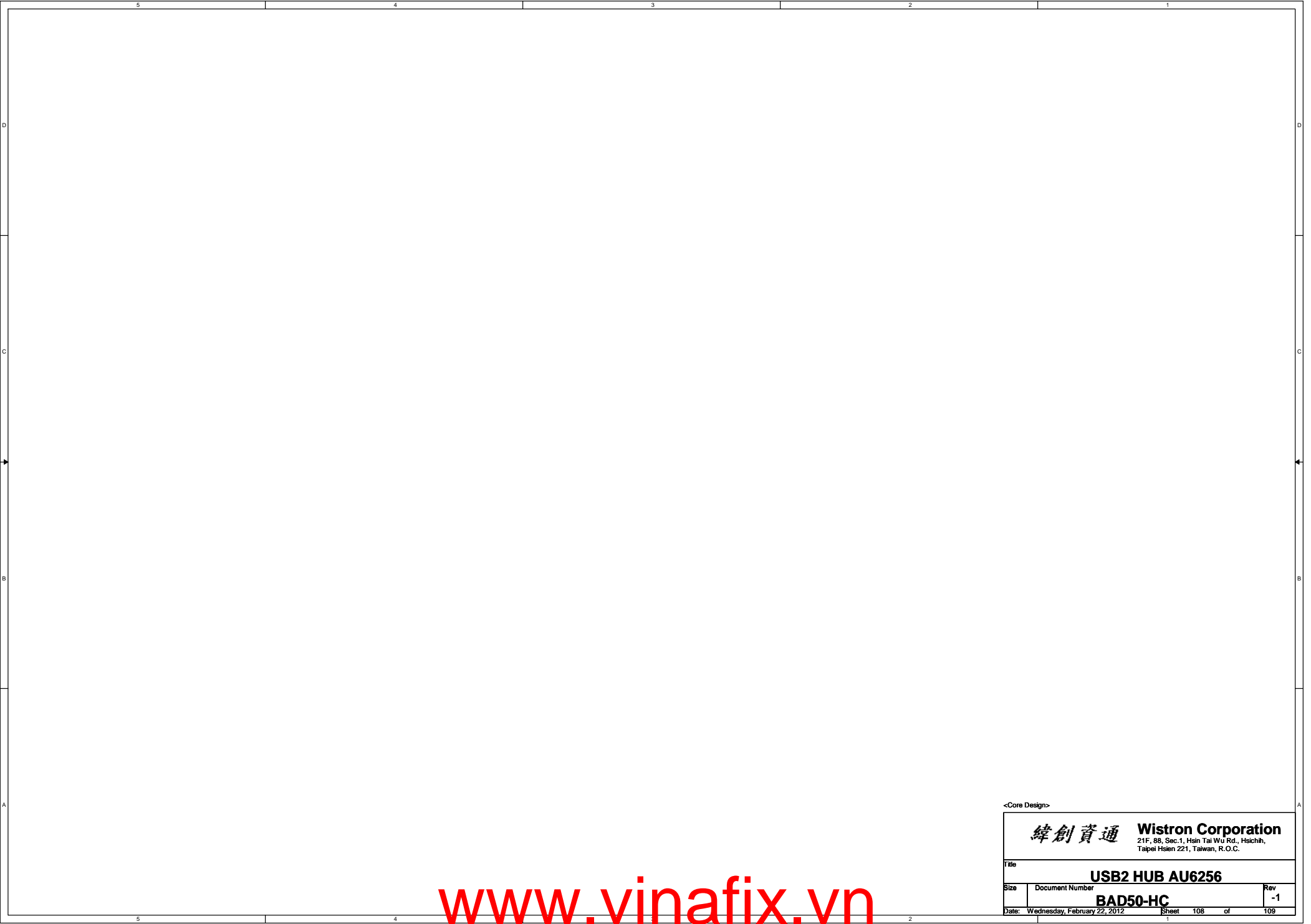
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Title		
LAN SWITCH		
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<p>Title</p>	
<p><b>USB charger</b></p>	
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Date:	Rev
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Title

USB2 HUB AU6256

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I2C mode  
To USB BD

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Title			
<b>USB30 re-driver</b>			
Size B	Document Number		Rev
	<b>BAD50-HC</b>		<b>-1</b>
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